SIEMENS

ICs for Telecommunications

Data Book 1983/84

Siemens Aktiengesellschaft

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* Advance information
▼ New type

1.1 Type designation code for ICs

The IC type designations are based on the European code system of Pro Electron. The code system is explained in the Pro Electron brochure D 15, edition 1982, which can be obtained from: Pro Electron
Boulevard de Waterloo 103
B-1000 Bruxelles

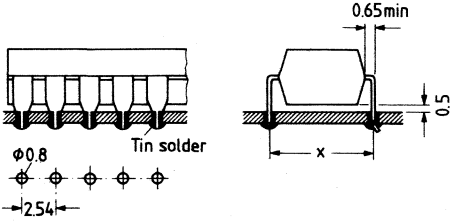
1.2 Mounting instructions

1.2.1. Plastic and ceramic plug-in package

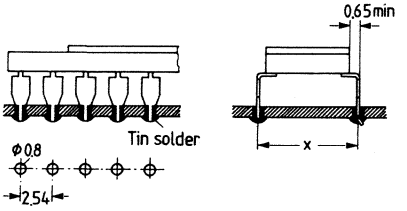
The plug-in packages are soldered to the PCB with the solder joints at the back of the board. The pins are bent down at an angle of 90°. They fit into holes of 0.7 to 0.9 mm diameter, spaced at an equal distance of 2.54 mm. The dimension × is shown in the corresponding package outline drawing.

The bottom of the package does not touch the printed circuit board after insertion, because the pins have shoulders just below the package (see figure).

After inserting the package into the printed circuit board, two or more pins should be bent at an angle of approximately 30° relative to the printed circuit board so that the package need not be held down during soldering. The maximum permissible soldering temperature for iron soldering is 265°C (max. 10 s) and for dip soldering 240°C (max. 4 s).



Plastic plug-in package



Ceramic plug-in package

Dimensions in mm

1.2.2 Ultrasonic cleaning of ICs

Freon and isopropyl alcohol (trade name 2-propanol) may be used as solvents. These solvents may also be used for plastic packages, as they are compatible with the plastic material. An ultrasonic bath in full-wave rectified operation is recommended due to the resulting low degree of component stress.

The following ultrasonic limits are permissible:

Sound frequency	$f > 40$ kHz
Duration	$t < 2$ min.
Sound pulse pressure	$p < 0.3$ atü
Sound power	$N < 0.5$ W/cm^2/litre

1.3 Assembly instructions for MICROPACKs

1.3.1 Delivery package

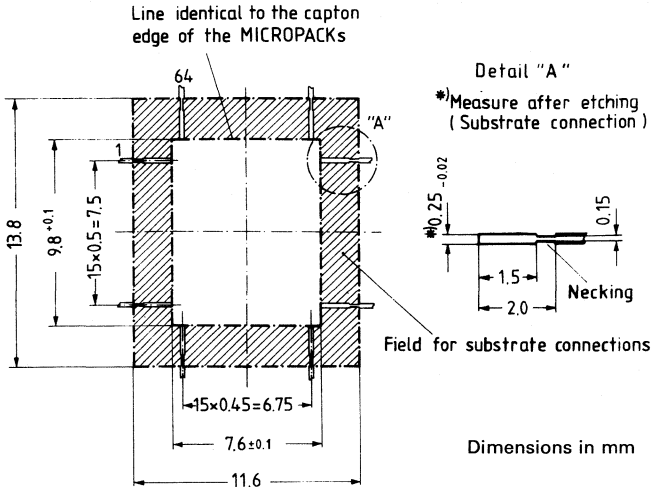
The MICROPACK PSB 7510 is generally delivered on metal film spools in metal cans. For prototypes, the IC can also be packed individually. MOS handling is necessary.

1.3.2 Substrate connections

For assembly of the MICROPACK, the connection points on the substrate must be coated with solder. This can be achieved by:

- Galvanic deposition and melting
- Screen printing and melting
- Dip or wave tinning

Solder tin compositon: Sn 60 / Pb 40
Thickness of the layer: approx. 15 µm (after melting)



Note: Necking of the connection leads is not required in the case of galvanically deposited Sn/Pb and subsequent melting.

1.3.3 Assembly recommendations

All assembly recommendations are valid for the following substrate materials:

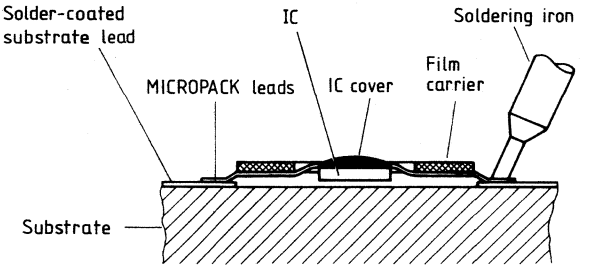
- Epoxy resin
- Hard-paper
- Ceramic (thick- thin-film)
- Flexible materials, as for example polyimide
- Glass

I. Prototypes and small quantities
(e.g. up to approx. 1.0/year)

Recommended processing method:

Manual soldering with mini soldering iron

Principle



Required equipment and accessories

- Devices for cutting and punching (only when processing from tape)
- Forming tools
- Temperature-regulated miniature soldering iron, certified for the soldering of MOS components
- Stereo microscope (magnification 6...40 ×)
- Suction tube or tweezers
- Hair brush
- Sodium-free flux according to DIN 8511 (e.g. pure colophonium dissolved in alcohol)
- Cleaning agents (if required): e.g. Freon T-P 35 and TF
- Bench top suited for the processing of MOS components

Soldering data

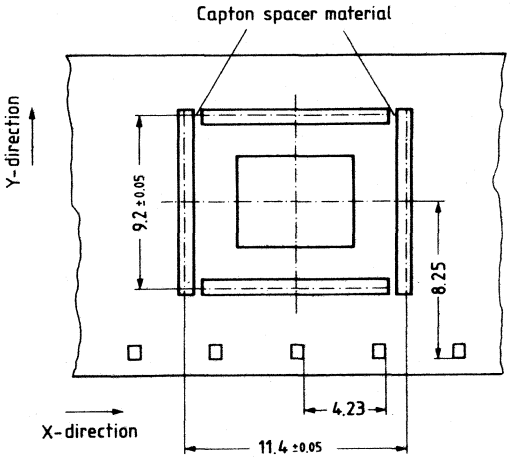
- Soldering temperature at the soldering iron tip: 230°C max.
- Soldering time: approx. 1 to 2 s

Procedure

Caution! The general rules for the processing of MOS components must be followed during all operations.

Cut MICROPACK leads free with hand tool (for components delivered on spools only).

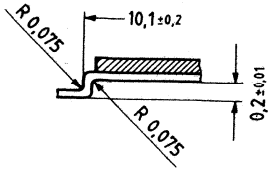
Cutting dimensions: 9.2 ± 0.05 mm × 11.4 ± 0.05 mm

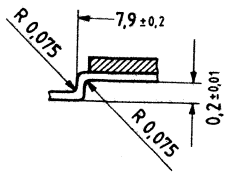


Caution! Only cut free along the dashed lines!
Do not cut the 4 capton spacers.

Form MICROPACK leads with hand tool.
(For the relief of mechanical strees when mounted)

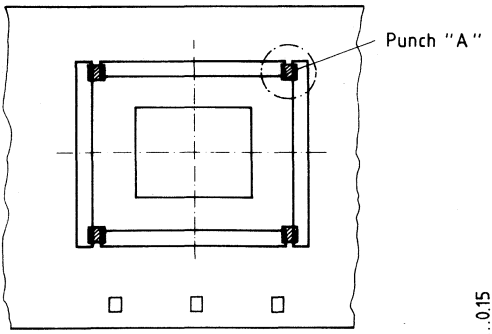
Forming dimensions

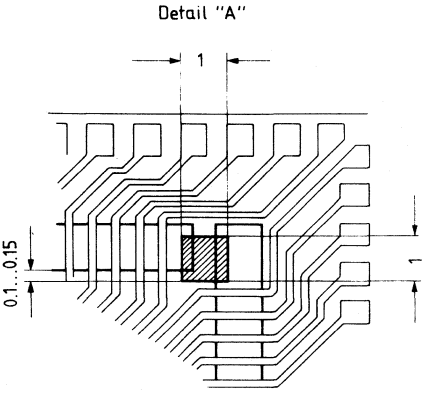




Dimensions in mm

Punch MICROPACK out of the film tape with hand tool (for components delivered on spools only)





Lay down the punched MICROPACK onto an electrically conductive surface vacuum pickup.

Coat the mounting points on the substrate with flux (with brush by hand).

Position the MICROPACK and adjust by hand under stereo microscope (approx. 5 to 10× magnification).

Solder the individual leads by hand with soldering iron under stereo microscope.

Important! First solder two opposite leads. This prevents a shifting of the MICROPACK during the soldering process.

Cleaning (if required)

Move the substrates one after the other for approx. 1 minute in T-P 35 and TF for example (no ultrasonic cleaning).

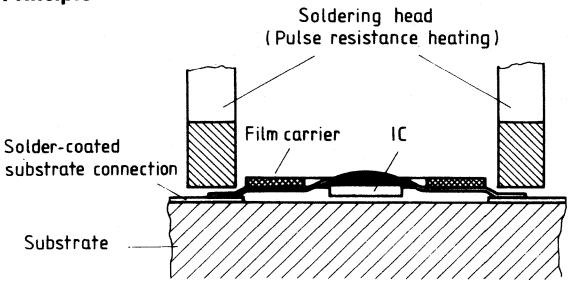
Place the cleaning substrates on an electrically conductive surface or in appropriate trays.

II. Medium quantities
(e.g. up to approx. 30.0/year)

Recommended assembling method:

Pulse soldering with manual device

Principle

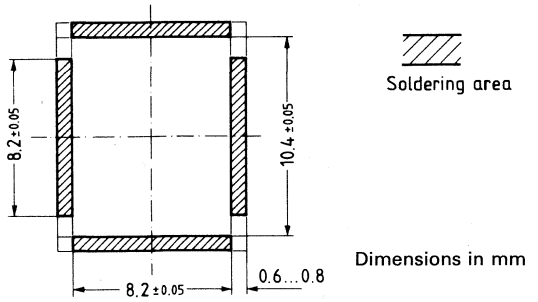


Required equipment and accessories

As in I., only instead of the soldering iron:

Pulse soldering device

Pulse soldering head (dimensions according to the drawing)



Head holder
Control device (temperature, time)
Substrate holder (with micro-manipulator, if necessary)
Stereo microscope

Soldering data

Soldering temperature at the pulse soldering head: 230°C max.
Soldering time: approx. 2 s plus an additional holding time of 1 s until the solder becomes solidified.

Procedure

As described in I. including the positioning of the MICROPACK onto the substrate and the adjustment.

Further steps

Position the substrate with the positioned MICROPACK onto the substrate holder of the pulse soldering device.

Lower, adjust and set down the soldering head onto the MICROPACK leads manually, then trigger the soldering pulse.

After the Pb/Sn solder becomes solidified (holding time, observation through stereo microscope) raise the soldering head and place the substrate onto an electrically conductive surface or in an appropriate tray.

Caution! Ceramic and glass substrates must be preheated and the stated temperatures must be maintained during the soldering process.

Ceramic: 150°C
Glass: 125°C

Neither preheating nor cooling may be sudden (danger of breakage).

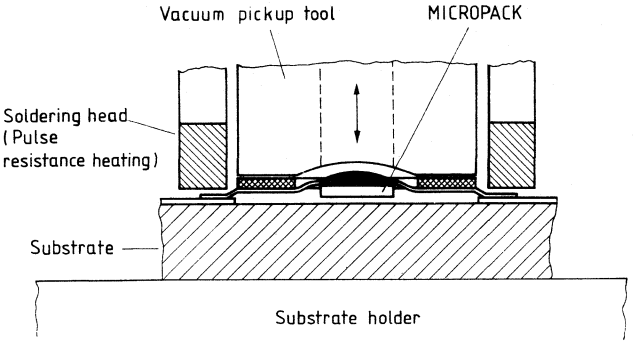
Cleaning (if required): as in I.

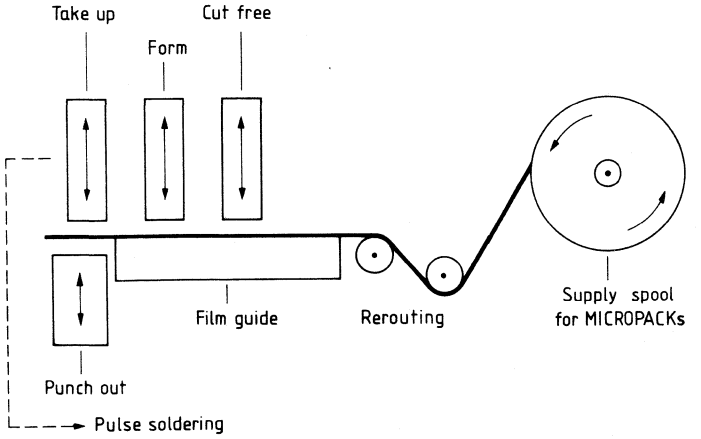
III. Large quantities
(e.g. approx. 30.0/year)

Recommended assembling method:

Semi-automatic pulse soldering

Principle





Required equipment and accessories

Semi-automatic pulse soldering device including tools for cutting, forming and punching.

Stereo microscope (magnification 6 to 40×).
Flux according to DIN 8511 (e.g. pure colophonium dissolved an alcohol).
Cleaning agents (if necessary): Freon T-P 35 and TF.

Soldering data

Soldering temperature at the pulse soldering head 230°C max.
Soldering time: approx. 2 s plus an additional holding time of 1 s until the solder becomes solidified.

Procedure

Position the supply roll in the pulse soldering device.

Coat the mounting positions on the substrate with flux by hand or machine.

Position the substrate onto the substrate holder.

Caution! Ceramic and glass substrates must be preheated and the stated temperatures must be maintained during the soldering process.

Ceramic: 150°C
Glass: 125°C

Neither preheating nor cooling may be sudden (danger of breakage).

Machine-cut, form, punch and pre-adjust the MICROPACK.

Fine-adjust with micro-manipulator (under the stereo microscope or on a monitor).

Pulse-solder by machine.

Place the substrate onto an electrically conductive surface or in an appropriate tray.

Cleaning (if required): as in I.

IV. Very large quantities
(e.g. approx. 500.0/year)

Recommended assembling method:

Fully automatic pulse soldering

Processing method as in III. but fully automatic

1.3.4 Final inspection

It is recommended, that a final visual inspection of the mounted MICROPACKs be included after soldering, respectively cleaning (under the stereo microscope, magnification 6 to 40×).

Important criteria

The solder transition between the MICROPACK leads and the substrate traces should be concave tapered.

The connections to the semiconductor IC must not be damaged.

The solder on all substrate leads must be visibly melted.

MICROPACK and substrate surface must not show signs of soiling after soldering, respectively cleaning.

1.3.5 Replacement

Experience shows that MICROPACKs can be replaced as many as five times depending on substrate material and layer construction.

Desolder the MICROPACK with miniature soldering iron or hot air gun and tweezers. The leads are heated to the melting point of the Pb/Sn solder and bent up with the tweezers.

Plane the mounting spots and recoat with flux.

Solder in a new MICROPACK using one of the methods described.

1.3.6 Manufacturers of assembly equipment for MICKROPACKs

The following companies supply equipment for manual, semi-automatic and fully-automatic assembling:

1. Weld-Equip Sales b.v.
Engelseweg 217
5705 AE Helmond
Netherlands

Fa. Weld-Equip Deutschland
Josef-Retzer Str. 47
8000 München 60
Phone (089) 883601/02

2. Fa. Farco Schweiz
Girardet 29
CH 2400 Le Locle
Phone (0041) 39318954

3. The Jade Coorporation
3063 Philmont Avenue
Huntingdon Vallery, Penna, 19006
USA

Jade Corp. USA, represented by Fa. BFI
Assar-Gabrielssonstraße 1 B
6057 Dietzenbach-Steinberg
Phone (06074) 27051

1.4 Processing guidelines for MOS circuits

1.4.1 General

MOS (**M**etal **O**xide **S**ilicon) technology components require careful handling, as the component can be destroyed by uncontrolled electrical charges, voltages of ungrounded equipment, overvoltage spikes or similar influences. The following handling guidelines must be adhered to, even if the components possess protective circuitry (e.g. protective diodes) at their inputs.
MOS components and other components with similar sensitivity that require handling accordance with this guideline, must be specially emphasized and identified in the appropriate factory specifications.

1.4.2 Scope

This guideline is valid for the storage, shipping, testing and processing of all types of MOS components, as well as fitted and soldered PC boards mounted with such components.

1.4.3 General handling

1.4.3.1 MOS components must remain in their containers until processed.

1.4.3.2 MOS components may only be handled at work stations specially equipped for this purpose.

1.4.3.3 Employees working at these work stations must wear the specified clothing and the bracelet required for grounding (refer to annex.).

According to the German (VDE) and international person protection regulations, at EGB work stations the conductive bench surfaces, floors and especially the grounding bracelets must be connected to ground potential through resistors $R_S > 50\ k\Omega$.

To ensure a sufficiently fast discharge of a charged person, the discharge resistance, e.g. at the bracelets including skin resistance, should not exceed $5M\Omega$.

The above requirements define the protective resistance range as

$$1M\Omega > R_S > 50k\Omega.$$

1.4.3.4 MOS components should only be removed from their package without touching the pins.

1.4.3.5 If short-circuit rings or straps are attached to the components, they should remain, if possible, until the component reaches the test area.

1.4.3.6 All MOS component transportation units and mounted PC boards must first be brought to the same potential by setting them down on the work station, or by being touched by the employee, before the individual MOS component may be touched.

1.4.3.7 Machines, tools or equipment, with which MOS components are processed or transported, must be conductive.

The metal machine parts, tools and equipment, that can be touched from the outside, are included in a potential compensation system that is connected to the MOS work station and ground, insofar as this is not contrary to VDE regulations (e.g. for tools, with low voltage transformers).

1.4.3.8 Sensitive PC boards, and those mounted with MOS components, must be handled in accordance with section 1.4.8.4.

1.4.4 Delivery, shipping

MOS components and PC boards mounted with MOS components must be shipped in clearly marked and suitable packing material, e.g. in conductive foam, in metal or plastic tracks fitted with an anti-static coating or with short-circuit connectors. Plastic rails may not be used more than 10 times. Additionally, the delivered packing, or the transportation units used in production, must bear a standardized label.

1.4.5 Storage

MOS components may only be stored in defined, marked areas. During storage, the components should remain in the packing material in which they were shipped. During repacking and removal from storage, section 3 must be complied with.
If smaller quantities are to be delivered, the individual components must be repacked into conductive transportation containers suited for MOS.

1.4.6 Transportation

MOS components may only be transported in containers or transportation carts reserved for MOS. The carts and containers for the individual components must be made of conductive material (steel rails or conductive plastic), or possess a conductive coating (conductive silver paint).

Transportation carts must be equipped with a sliding contact strap, touching the ground. These carts can be recognized by an orange marking (RAL 2004).

Transport containers painted orange (RAL 2004), labelled MOS, may only be used as containers for MOS components and for PC boards equipped with MOS components.
These containers must be lined with conductive foam rubber. Supplier is e.g. Canespa KG, Gutenbergstrasse 13, D-3005 Hemmingen 1, Designation of the foam rubber: electrically conductive special foam "Packing 2000".

1.4.7 Incoming inspection

Incoming inspection of MOS components should be kept to a minimum. If necessary, tests should be carried out in accordance with sections 3 and 9.

1.4.8 Materials and mounting

1.4.8.1 The work station at which MOS components and PC boards mounted with MOS components are to be handled, must be designed as shown in the annex.
The drive belts of machines used for MOS processing must be treated with antistatic spray (e.g. Anti-Static Spray 100 from the Kontaktchemie company), insofar as they get into contact with these components (e.g. bending and cutting machines, conveyor belts). It would be better, to avoid such contact.

1.4.8.2 If MOS components are to be soldered in or out by hand, only suitable soldering irons must be used ref. to section 1.4.3.7 e.g. ADCOLA L101 of the Polytronik GmbH, Quagliostrasse 6, D-8000 Munich 90, Tel.: (089) 661233, or soldering irons with protective in insulation from the ERSA and ZEVATRON companies.
Do not use soldering irons with thyristor regulation – voltage spikes!
Desoldering equipment for freeing the holes by suction, e.g. ERSA Soldapullt, must be equipped with metal tips.

1.4.8.3 Soldered PC boards, mounted with MOS components, which are endangered during transportation, must be named by the technical order; inclusion in the factory specifications is required.
They must be transported in appropriate and marked transportation equipment, ref. to section 1.4.6. If there is no such note in the factory specifications, no precaution need be taken.

1.4.8.4 All MOS components must be processed in accordance with section 1.4.3. Short-circuit rings or short-circuit straps must not be removed during the assembly of the PC board, if they can easily be removed in the test area.
Traces and MOS components on soldered PC boards should not be handled.

1.4.8.5 The Statometer H1407 from Herfurth GmbH, P.O. Box 13249, D-2000 Hamburg 50 is suited for the contactless measurement of electrostatic charges.

1.4.9 Electrical test

1.4.9.1 The components must be processed in accordance with section 1.4.3 and 1.4.8. Before the fitted and soldered PC boards are tested, any attached short-circuit ring should be removed.

1.4.9.2 Test socket must be voltage-free during the plug-in or removal of individual components or PC boards, unless otherwise stated in the factory specifications. It must be assured that the test devices do not generate voltage spikes when they are turned on and off during operation or in case of a failure of the mains fuse, or if other fuses fail.

1.4.9.3 Signal voltages may only be applied to MOS circuit inputs at the same or after the supply voltage is applied. They must be removed before or at the same time as the supply voltage is turned off.

1.4.9.4 The information in the appropriate data books must be observed.

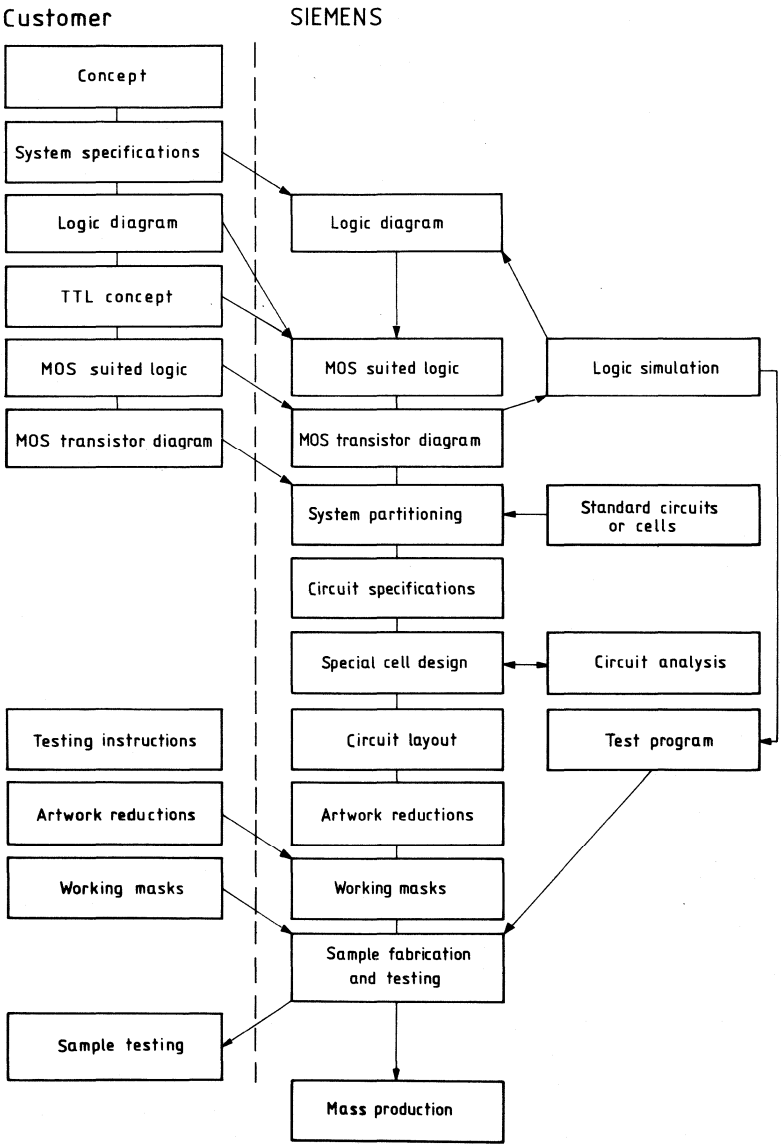
1.4.10 Packaging

The packaging of PC boards equipped with MOS and soldered must be carried out at a work station as shown in the annex. Any attached short-circuit rings must be removed.
Recommended packaging: wrapping the mounted PC boards in conductive material, e.g. aluminium foil and packing them into suitable cardboxes or packaging containers lined on both sides with conductive foam material.

1.4.11 Binding character

The above guidelines can be complemented at any time by the users, or changed on their own responsibility, respectively.
Internal factory regulations must be observed.

1.4.12 Possibility of cooperation between Siemens and the customer at the various stages of an MOS circuit development



1.5 Data classification

Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Electrical characteristics

The electrical characteristics include the guaranteed tolerances of the values, which are maintained by the integrated circuit in the specified operating range.
The typical characteristics are mean values which are expected from production. Unless otherwise specified, the typical characteristics apply to T_{amb} = 25°C and the specified supply voltage.

Operating data

In the operating range, the functions shown in the circuit description will be fulfilled.

1.6 Quality specifications

The delivery quality of integrated circuits is specified as follows:

1.6.1 Maximum ratings and tolerance limits of the characteristics

1.6.2 Sampling inspection, AQL values (acceptable quality level)

Inspection by attributes* is based on the identical sampling inspection plans DIN 40080, (or) ABC Standard 105, inspection level II, normal inspection.

A delivery lot for which the defect percentage for a certain characteristic is equal or less than the specified AQL value, will most propably (more than 90%) be accepted in the appropriate sampling inspection.

The average defect percentage of delivered products lies, in general, clearly below the AQL value.
Only the number of defective units is evaluated in the sampling inspection.

1.6.3 Defects

A defect exists if a component characteristic does not correspond to the specifications in the data sheet.

The defects are classified as total defects, defects in the electrical features, and defects in the mechanical features. Unless otherwise agreed upon, the AQL values in section 5 apply to the various defect types.

* Inspection for a characteristic for which only 2 mutually exclusive properties are specified (good/bad).

1.6.4 Classification of defects

Total defect:
- open contact or short circuit within a specified temperature range
- no marks, or wrong type and/or direction of mark
- wrong marking of pin 1
- mixed with wrong versions
- components not aligned within one rail
- broken package and/or pins

Defect in the electrical features:
- exceeding electrical maximum ratings

Defects in the mechanical features:
- defects on the package surface
- type marking hard to identify
- bent pins
- wrong dimensions

1.6.5 AQL table

Defect type	AQL values Bipolar IC	MOS IC
Total defect (mechanical and electrical)	0.1	0.25
Sum of electrical defectives	0.4	0.4
Sum of mechanical defectives	0.4	0.4
AQL value 1.5 applies to switching times		

1.6.6 Incoming inspection

The tests carried out by the manufacturer are intended to render expensive incoming inspection by the user unnecessary. If the user, however, wants to carry out such inspections, we recommend the use of a sampling inspection plan as described in section 1.6.7.
The test method used must be agreed upon between customer and supplier.

The following information is required to adjust a possible claim:
test circuit, sample size, number of defective items found, sample of evidence, packing list.

1.6.7 Sampling inspection plan for normal inspection

in accordance with DIN 40080 or ABC-Std 105 D, inspection level II

Lot size	Sample size	AQL-value										
		0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1
9 to 15	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↕
16 to 25	5	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓
26 to 50	8	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2
51 to 90	13	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3
91 to 150	20	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4
151 to 280	32	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6
281 to 500	50	↓	↓	↓	0 1	↕	↓	1 2	2 3	3 4	5 6	7 8
501 to 1200	80	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	0 1	↕	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑
35001 to 150000	500	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑
150001 to 500000	800	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑
500001 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑

A = Acceptance number, i.e. the maximum number of defective sample units up to which the lot is accepted.

R = Rejection number, i.e. the number of defective sample units which must at least be found for the lot to be rejected.

Additional requirement

As the combination "Acceptance 0 and Rejection 1" has a low degree of significance, the next larger size should be sampled.

1.6.8 Quality assurance

High quality and reliability is the result of of careful dimensioning of highly developed manufacturing processes and a quality assurance system of several stages.

The Siemens quality assurance system for integrated circuits (SQS-IS) ensures to achieve the necessary quality goals and continually initiates further quality improvements. It comprises

- qualification assessment of new processes and products,
- quality controls during manufacturing,
- release tests on production lots after essential manufacturing sections,
- recording of quality and reliability of the final product,
- evaluation of experience,
- failure analysis.

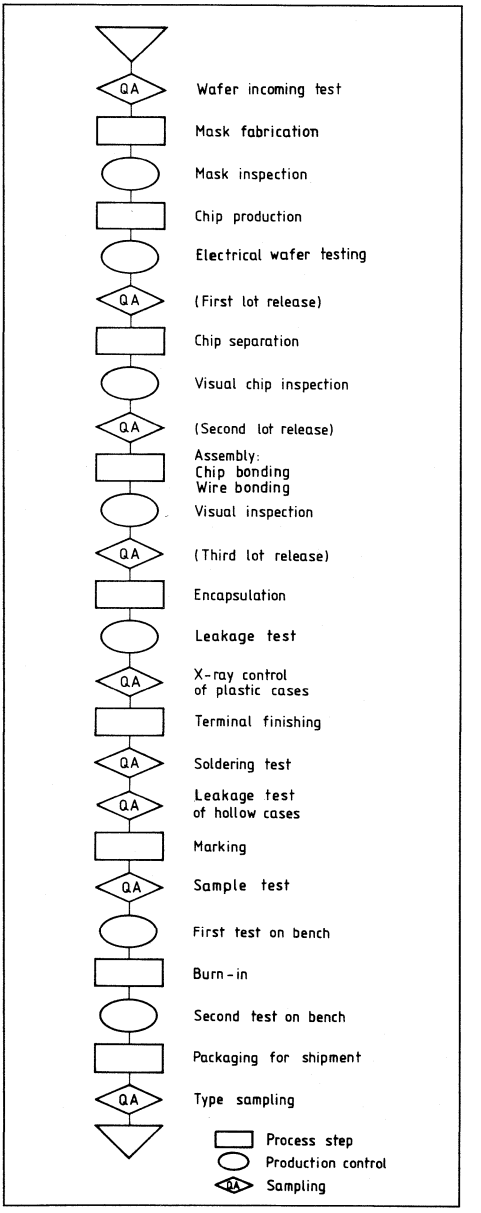
From the application requirements quality classes are deduced, each of which is determined by quality assurance measures as follows:

Class QC
for all technical applications with commercial reliability requirements,

Class QB
for applications requiring high reliability, as in control engineering, data processing, or communications engineering,

Class QA
for very high reliability applications comprising the ability to meet extreme demands like long life with critical functions. For this class, usually special agreements between the component user and manufacturer will be needed.

In detail, the quality class of the component is selected by evaluating the reliability of the functional unit considered. For classes QB and QA, additional inspections and controls during the manufacturing process and – if required by the user – special tests are carried out before delivery. A usual measure to reduce early failures is an electro-dynamic burn-in at maximum conditions.



Quality assurance steps during the production process

Reliability

Reliability of integrated circuits is the ability to perform the required functions under stated conditions for an extended period time. A measure for the reliability is the failure rate. It indicates the failure probability at an assumed time. The failure rates are calculated on the basis of sampling results obtained from specimens submitted to stresses – under tightened conditions for time acceleration purpose.

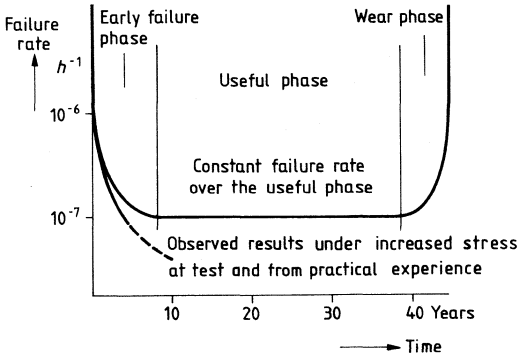
The electrical test is carried out periodically about every three weeks. The results are cumulated, transferred into operational conditions and completed by relevant practical experience. Thus the empirical values for the failure rate are obtained.

The "tub curve" diagram for expressing the time-dependent response of the failure rate, as known from other fields, generally applies also to the components of microelectronics. It indicates the phase of early failures caused by a small number of components, succeeded by a range of low and practically constant failure rate over an extended time period, the so-called useful phase. The following wear phase was not yet considered for integrated circuits. The system reliability predictions are based on the level of the useful phase.

Cooperation with the customer

Besides general quality assurance following the above stated fundamentals, optimization of the quality in cooperation with the customer plays an important role as the user needs a quality level perfectly adapted to his project. In connection with the use, application-specific failure causes may occur, which must be detected together with the customer and, consequently, may lead to circuit design changes or require special test criteria to be observed by the manufacturer.

Comparison of theoretical and actual failure rate.
Failure rate vs. time



1.7 Summary of the symbols

b	Pulse duration
B	Current gain
B	Bandwidth
BI	Input of output amplifier
BO	Output of output amplifier
C	Capacitance
C_I	Input capacitance
C_{ICL}	Input capacitance of the clock input
C_{OL}	Load capacitance at output
DI	Data input
DO	Data output
E	Enable
F_I	Input load factor
F_O	Output load factor
F_{OH}	Output load factor, H signal
F_{OL}	Output load factor, L signal
f_I	Input frequency
f_{CL}, f_Φ	Clock frequency
f	Maximum counter frequency
I_{DD}	Drain supply current
I_I	Input current
I_{IH}	H input current
I_{IL}	L input current
I	Input
I1	Input 1
I2	Input 2
I	Input bias current
I_{OO}	Output offset current
I_O	Short-circuit output current
I_{OH}	H output current
I_{OL}	L output current
I_{SH}	H supply current
I_{SL}	L supply current
MO	Mixer output
O_S, GND	Ground, earth
P_{tot}	Total power consumption
P_O	Output power
CLK	Clock
O	Output
$\overline{O}$	Output, inverted

R	Resistance
R_F	Input resistance
R_G	Generator resistance
R_I	Input resistance
R_C	Collector load resistance
R_L	Load resistance
R_P	Adjustment resistance
R_{thJA}	Therminal resistance (Junction to ambient)
R_{OH}	H output resistance
R_{OL}	L output resistance
R_O	Load resistance at output
T_{amb}	Ambient temperature
T_{stg}	Storage temperature
T_{case}	Case temperature
T_j	Junction temperature
TC	Temperature coefficient
t_d	Pulse delay time
$t_{DHL\ O}$	Delay time of the HL transition of the output signal
$t_{DLH\ O}$	Delay time of the LH transition of the output signal
t_{DLH}	Delay time
t_H	Hold time
t_I	Input pulse duration
t_n	Bit time before clock pulse
t_{n+1}	Bit time after clock pulse
t_P	Average signal propagation time
t_{SYD}	Delay time
t_{CLY}	Clock period
t_{PHL}	Signal propagation time (from H to L)
$t_{PHLR,S}$	Signal propagation time (set, reset input)
t_{PD}	Pair-delay time
t_{pR}	Reset pulse duration
$t_{PR,S}$	Average signal propagation time (set, reset input)
t_{pS}	Set pulse duration
t_d	Key debounce time
t_p	Key depression period
t_{pC}	Counting pulse duration
t_T	Transmission time – t_r rise time, t_f fall time
t_r	Recovery time
t_S	Setup time
t_O	Output pulse duration
t_{THL}	Signal transition time (from H to L)
t_{TLH}	Signal transition time (from L to H)
$t_{THL\ O}$	Signal transition time H-L of the output signal
$t_{TLH\ O}$	Signal transition time L-H of the output signal

t_{SH}	H setup time
t_{SHI}	H setup time, left shift pulse
t_{SHr}	H setup time, right shift pulse
t_{SL}	L setup time
t_{SLI}	L setup time, left shift pulse
t_{SLr}	L setup time, right shift pulse
$t_{WH\ I}$	Pulse width of the H input signal
$t_{WL\ I}$	Pulse width of the L input signal
$t_{THL\ I}$	HL transition time of the input signal
$t_{TLH\ I}$	LH transition time of the input signal
$t_{WH\ O}$	Pulse width of the H output signal
t_W	Pulse width
V	Voltage, general
V_S	Supply voltage
V_{nm}	Noise margin
V_{BB} / V_{EE}	Negative supply voltage
V_{CC}	Positive supply voltage
V_{SS}	Substrate supply voltage
V_{DD}	Drain supply voltage
V_{GG}	Gate supply voltage
V_{IH}	H input voltage at information input
V_{IL}	L input voltage at information input
V_{OH}	H output voltage
$\overline{V_{OH}}$	Inverted output voltage V_{OH}
V_{OL}	L output voltage
$\overline{V_{OL}}$	Inverted output voltage V_{OL}
V_{DI}	Differential input voltage
V_{cm}	Input common mode voltage
V_n	Noise voltage
V_F	Functional voltage range
V_I	Input voltage at information input
V_R	Reset voltage
Z_I	Input impedance
Z_O	Output impedance

ICs for Telephone Sets

Tone Ringer

PSB 6520 (S 124 A)

Preliminary data

Bipolar circuit

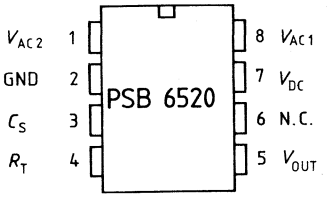
Type	Ordering code	Package outline
PSB 6520	Q67000-Z18	DIP 8

The PSB 6520 bipolar integrated circuit, in conjunction with an electro-acoustic converter, replaces the mechanical bell in the telephone set **(fig. 1)**. The component generates two periodic switchable tone frequencies that can either drive a piezo-ceramic converter directly, or a loudspeaker.

Special features

- Integrated bridge rectifier allows direct input via call signal (AC voltage)
- Low current consumption (several tone ringers can be connected in parallel)
- High noise immunity due to built-in voltage-current hysteresis
- Direct replacement of the mechanical bell requiring 4 additional external components and an acoustic converter
- Two-tone frequencies, switched internally
- Tone and switching frequencies adjustable by means of a resistor and a capacitor
- Overvoltage protection in accordance with VDE 0433 (2 kV-10/700 µs)

Pin configuration
top view

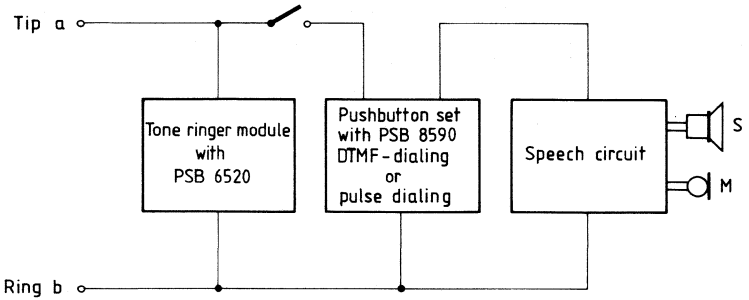


Pin designation

Pin No.	Symbol	Description
1	V_{AC2}	AC voltage input **(fig. 3)**
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	V_{OUT}	Output voltage
6	N.C.	Not connected
7	V_{DC}	Connection for smoothing capacitor 10 µF (internal supply voltage)
8	V_{AC1}	AC voltage input

Figure 1

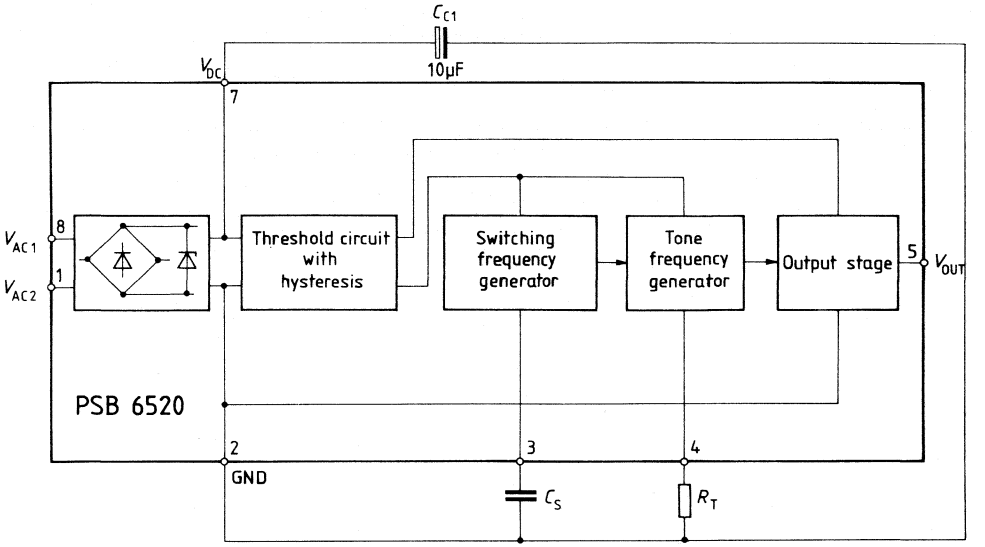
Block diagram of a standard electronic telephone set
(Pushbutton set and speech circuit connected in series)



Functional description

The tone ringer PSB 6520 is designed for use as an electronic bell in a telephone set. **Figure 2** shows the block diagram and **figure 3** the application circuit of the PSB 6520 in the telephone set.

Figure 2
Block diagram of the PSB 6520 tone ringer



The IC contains an oscillator which generates a square wave voltage. The frequency of this voltage is periodically switched by a second oscillator back and forth between two basic values having a ratio of 1:1.38. The basis frequency f_{1T} is adjusted by the resistor R_T and the switching frequency f_S by the capacitor C_S **(fig. 12 and 13)**.

Tone frequencies f_{1T} (Hz) $= \frac{2.72 \times 10^4}{R\ (k\Omega)} \pm 10\%$

f_{2T} (Hz) $= 0.725 \times f_{1T} \pm 2\%$

Switching frequency f_S (Hz) $= \frac{750}{C\ (nF)} \pm 15\%$

Good frequency stability is achieved by means of internal temperature compensation.

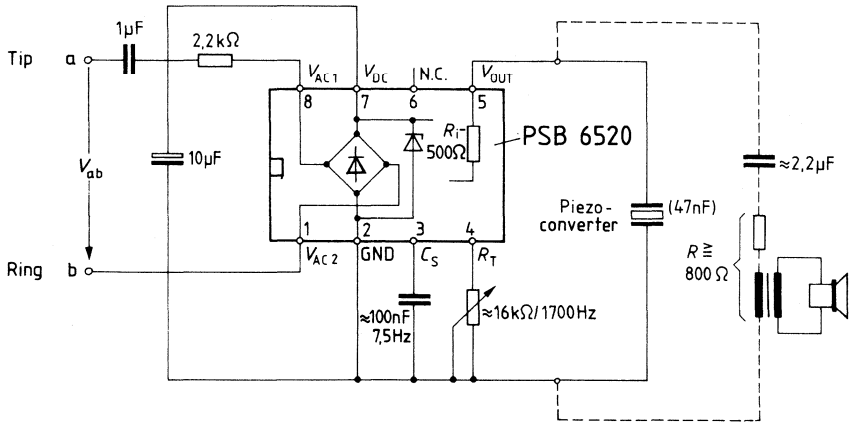
An output stage increases the generated tone voltage and transfers it to a piezo-resonator via an internal resistor. An electro-dynamic converter can be similarly driven, but must be matched to the internal resistance of the output stage **(fig. 6, 7, 8 and 12)** with a transmitter.

An integrated bridge rectifier enables direct input via the call AC voltage signal (tip (a), ring (b)) wires or via DC voltage (independent of polarity). A DC voltage supply without use of the integrated bridge is possible via the connections 2 and 7. In conjunction with a Z diode, the bridge rectifier serves simultaneously as an overvoltage protection.

The application circuit shown in **figure 3** can handle overvoltages occurring due to lightning strikes between terminals a and b according to the VDE 0433 standard, or the occurrence of an AC voltage of 110 V/50 Hz over a period of 30s, thus avoiding the possibility of any damage to the IC. The threshold circuit with high threshold voltage and hysteresis is designed to prevent activation **(fig. 4)** of the IC due to noise pulses.

Figure 3

PSB 6520 application circuit for telephone sets



The characteristic curves from **figure 4** to **figure 6** show the relationship between current consumtion, supply voltage, output current, output power, output resistance and AC calling voltage.

Maximum ratings		Test conditions	Min.	Max.	Unit
Supply voltage	V_{DC}	10 ms		28	V
Voltage pin 3 to pin 2	$V_{3,2}$			5.5	V
Voltage pin 4 to pin 2	$V_{4,2}$			7	V
Noise current into the output	$I_{N\ OUT}$	30 µs/mark to space ratio 1 : 100		20	mA
Storage temperature	T_{stg}		−40	125	°C
Operating range					
Calling voltage	V_{ab}	f = 50 Hz Test circuit **figure 3**			
		Continuous operation		90	V_{rms}
		5 s operation/ 10 s pause		110	V_{rms}
Supply voltage	$I_{=}$	DC supply current		22	mA
Tone frequency	f_{1T}	Validity of the formula f_{1T}	0.1	15	kHz
Ambient temperature	T_{amb}		−20	70	°C

DC characteristics		Test conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DC}	−20°C to 70°C			26	V
Current consumption without load	I_{DC}	V_S = 8.8 V to 26 V, 25°C		1.5	1.8	mA
Hysteresis circuit						
Threshold voltage	V_{th}	−20°C to 70°C	12.2	12.6	13.0	V
Switch-OFF voltage	V_{OFF}	−20°C to 70°C	8.0	8.4	8.8	V
Initial resistance	R_{INI}	25°C	6.4	7.4	8.5	kΩ
Voltage[1] deviation at output pin 5 referred to pin 2	V_{OUT}	25°C		V_S−3		V
Short-circuit current	I_{OUT}	U_S = 20 V, 25°C		35		mA
Tone frequency temperature coefficient	TC	−20°C to 70°C		8×10^{-4}		K^{-1}

[1] An internal resistor of 500 Ω is connected before the output.

Characteristic curves

Figure 4
Current consumption versus supply voltage V_{DC} without output load

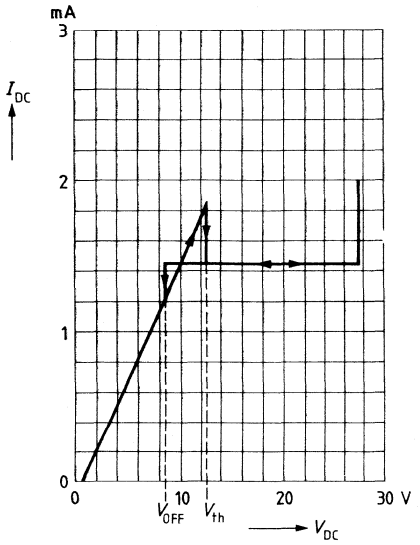


Figure 5
Amplitude of output current versus supply voltage V_{DC} in the case of short-circuit

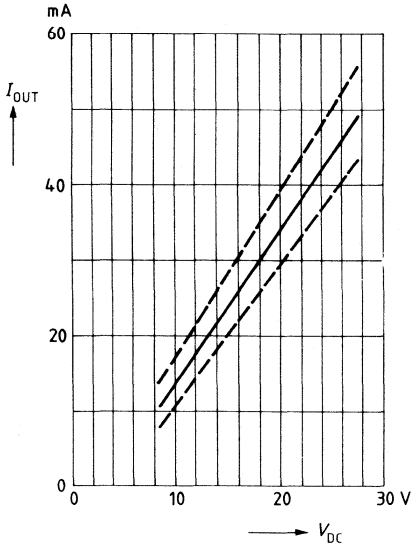


Figure 6
Output power versus load resistance R_{OUT} (ohmic)

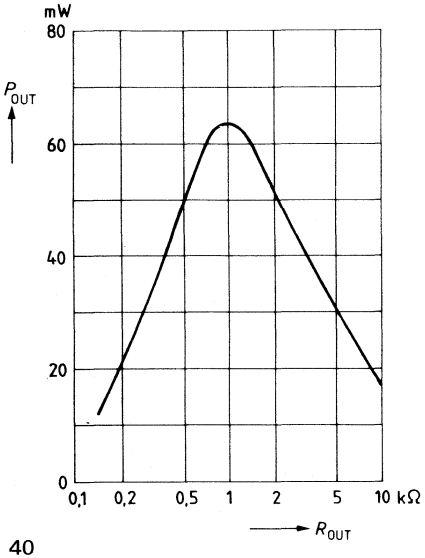


Figure 6.1

Test circuit to determine output power at different load resistances

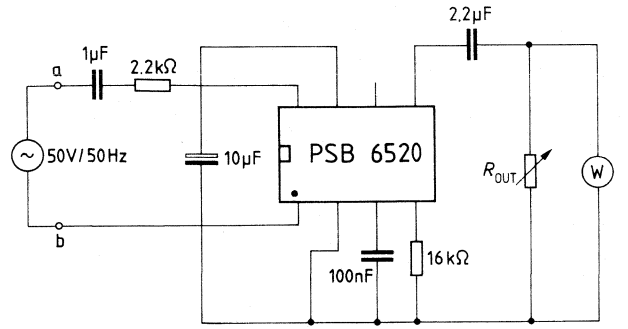


Figure 7.1

Test circuit to determine output power for a variable call voltage V_{ab}

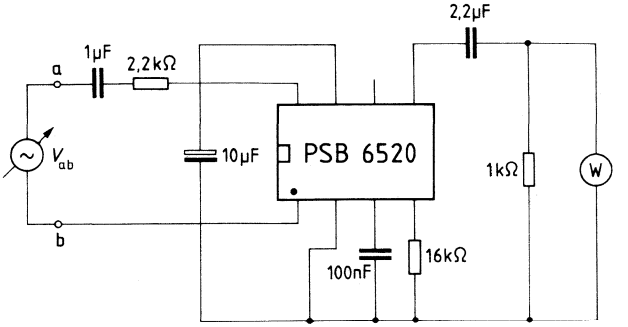


Figure 7

Output power versus call voltage for power matching

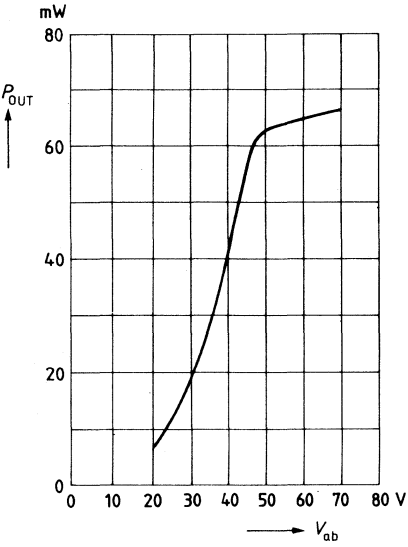


Figure 8

Effective output resistance versus call voltage V_{ab}

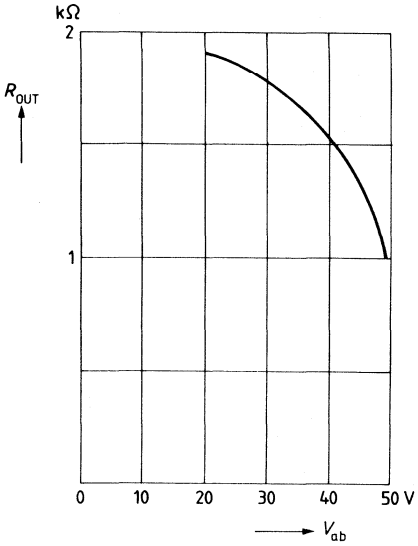
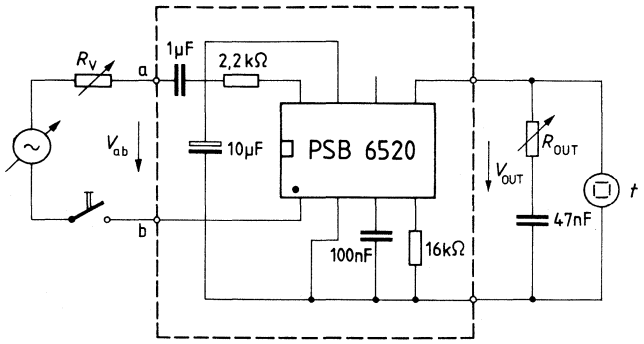


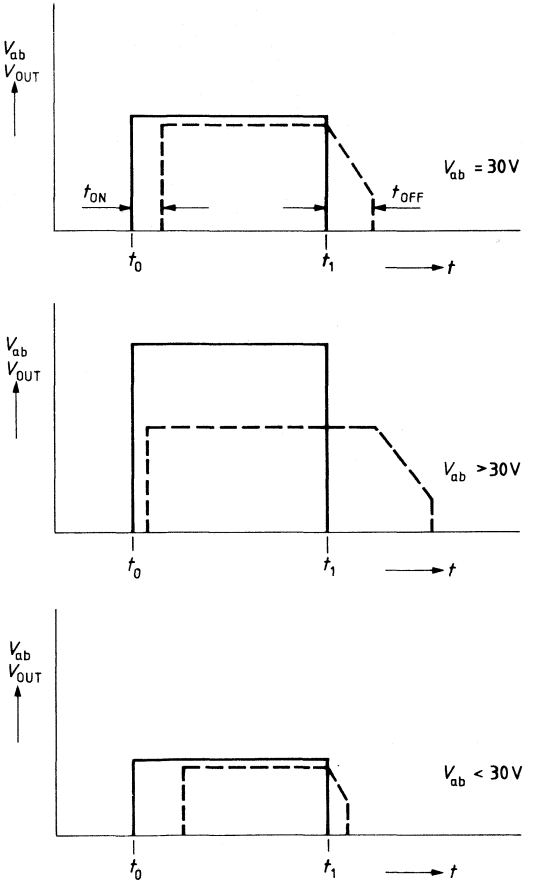
Figure 9

Test circuit to determine delay times



Delay times

Figure 9.1
Delay times t_{ON}, t_{OFF} versus V_{ab}



———— Effective value of input signal (call voltage V_{ab})
---------- Effective value of output signal (output voltage V_{OUT})
$t_1 - t_0$ Time duration of applied call voltage V_{ab}

Figure 10

Switch-on delay time t_{ON} versus V_{ab} (independent of R_{OUT})

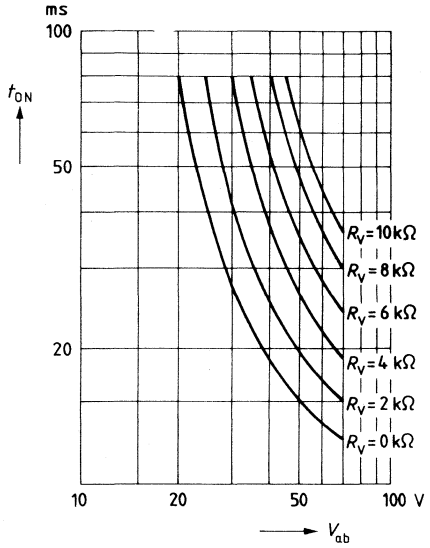


Figure 11

Switch-of delay time t_{OFF} versus V_{ab} (independent of R_V)

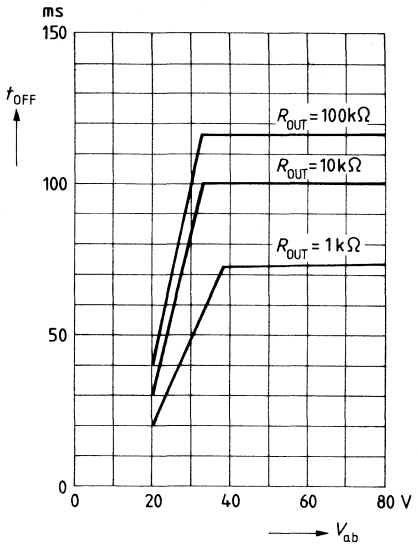


Figure 12

Frequencies f_{1T} and f_{2T} versus resistor R_T.

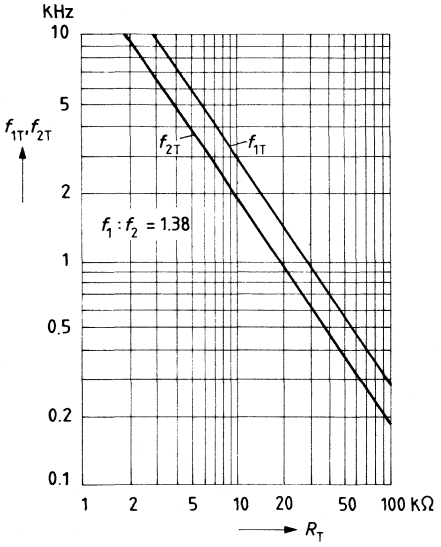
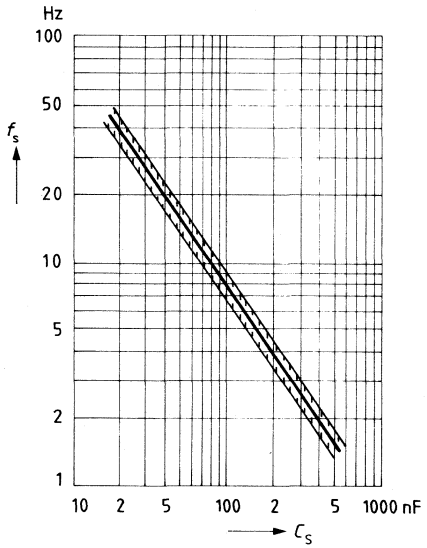


Figure 13

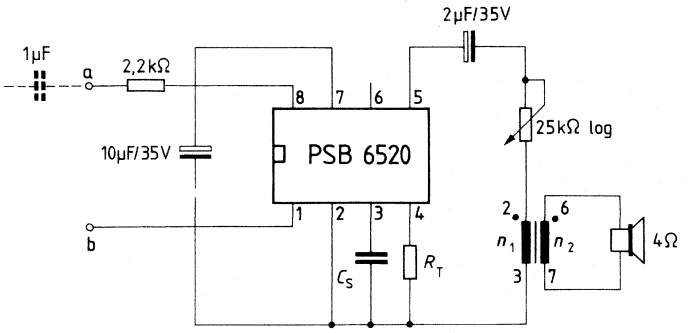
Switching frequency versus capacitor C_S



Recommended circuitry of PSB 6520 with a small loudspeaker

Figure 14

Matching a 4 Ω loudspeaker to the PSB 6520



Transformer

Pot core: Ordering code B 65651–K–R30
(18 × 11)

Material: N30, A_L = 5600 nH/W^2

Bobbin: Ordering code B 65652–B–T1

Windings: n_1 = 800, d_1 = 0.08 mm CuL
n_2 = 50, d_2 = 0.4 mm CuL

Dual-Tone Multi Frequency Generator

PSB 8590
(S 359)

Preliminary data

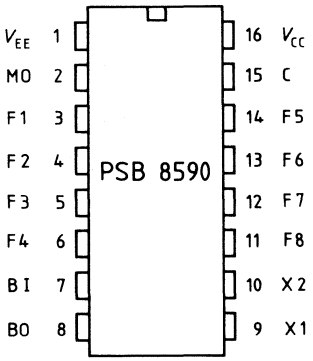
Bipolar circuit

Type	Ordering code	Package outline
PSB 8590	Q67000-Y477	DIP 16

Features

- CEPT-compatible
- Direct line feeding
- High frequency accuracy (deviation less than 0.4%)
- Standard low cost clock crystal 4.19 MHz
- Operation with either single contact or 2–of–8 keypads
- Dual-tone as well as single-tone capability
- Multi-key lockout and debouncing
- Binary interface mode
- Power dissipation limited by internal thermal overload protection

Pin configuration
top view

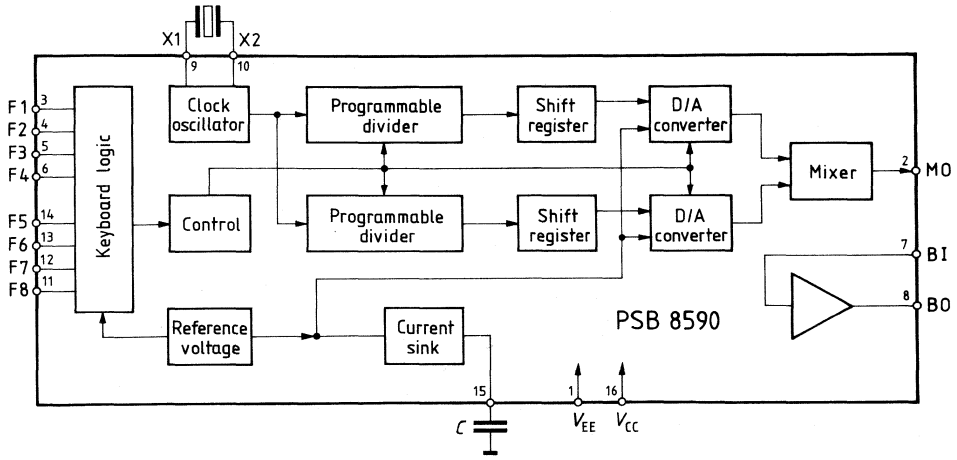


General description

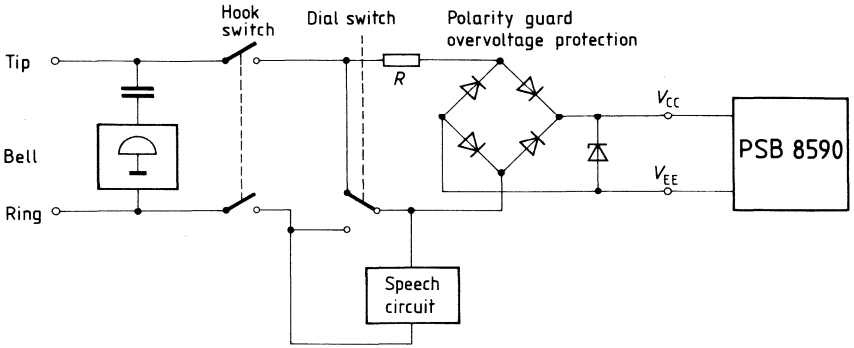
The DTMF generator PSB 8590 is a monolithic IC using the I^2L technology. It provides all dual-tone multifrequency (DTMF) pairs required in tone dialing systems. The eight different audio output frequencies are generated from an on-chip reference oscillator with an external low cost clock crystal 4.19 MHz. The internal temperature compensated voltage reference determines the audio output levels and it also controls the on-chip shunt regulator which provides the adaptation to different feeding conditions. In order to meet the CEPT recommendations an external 2-pole *RC* filter can easily be connected. A typical telephone application is shown in **figure 14.**

The PSB 8590 can interface directly to a single contact keypad. Furthermore, open collector outputs can control the PSB 8590 either in a BCD-mode or in a 2–of–8 keypad mode.

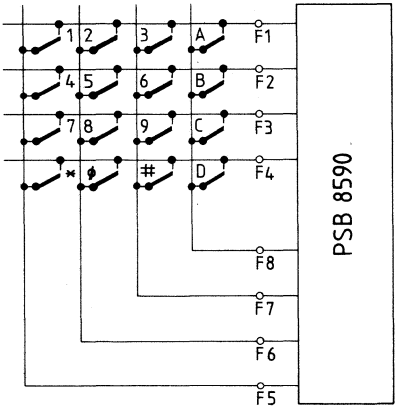
Block diagram



Connection to line



Connection to keyboard



The keys are debounced and electronically interlocked. If more than one key is pressed simultaneously, the key recognized as pressed first will be evaluated.

The requirements for the quality of contacts are:

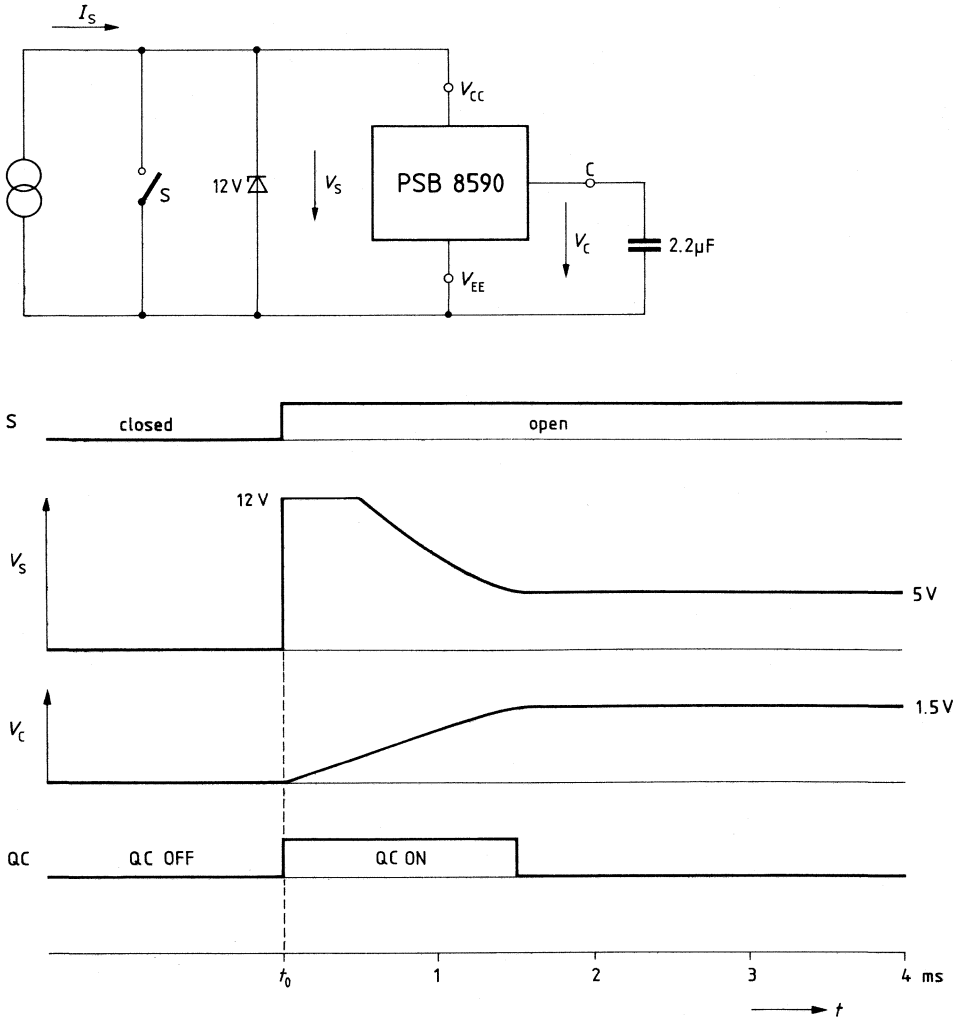
Open contact: Resistance $R_N > 50\ k\Omega$
Closed contact: Contact resistance $R_E \leqq 1\ k\Omega$ for $I = 100\ \mu A$

Functional description

1. Line adaptation

The DTMF generator PSB 8590 has an internal temperature-compensated voltage reference. This reference voltage controls a shunt regulator which sets the DC voltage $V_S = V_{CC} - V_{EE}$ to 5 V. The external filtering capacitor C gives the shunt regulator for frequencies above 300 Hz the behavior of a high impedance current sink. The shunt regulator includes a start-up circuit for the quick charging of the filtering capacitor (**fig. 1**). The shunt regulator can sink feeding currents up to 120 mA while the power dissipation is limited by internal thermal overload protection. If the chip temperature exceeds a preset value ($\approx T_j$ = 150°C, $P_V \approx$ 1 W), the filtering capacitor is discharged, the shunt regulator is switched off and the voltage V_S rises to the breakdown voltage of the external overvoltage protection network (**fig. 2**).

Figure 1
Tuning diagram of the quick charging circuit (QC) for the filter capacitor

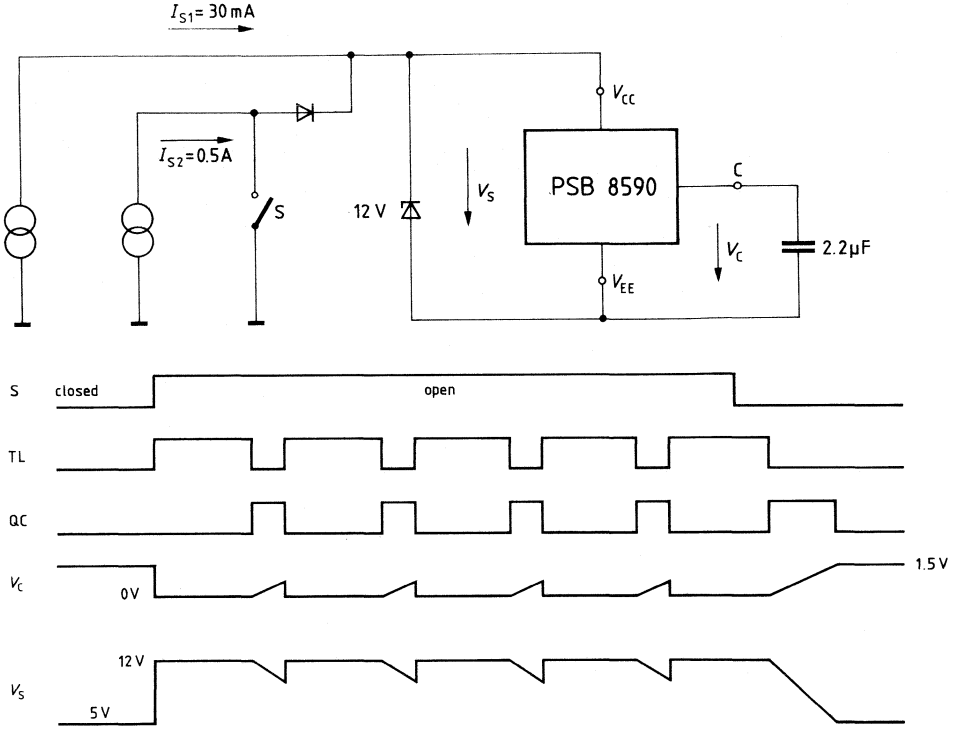


The control circuitry for the **q**uick **c**harging circuit has hysteresis with the following thresholds

QC	V_S	V_C
ON	X	< 0.7 V
ON	> 9 V	X
OFF	< 6.5 V	> 0.7 V

Figure 2

Output waveforms V_S during thermal limitation (TL) of the power dissipation

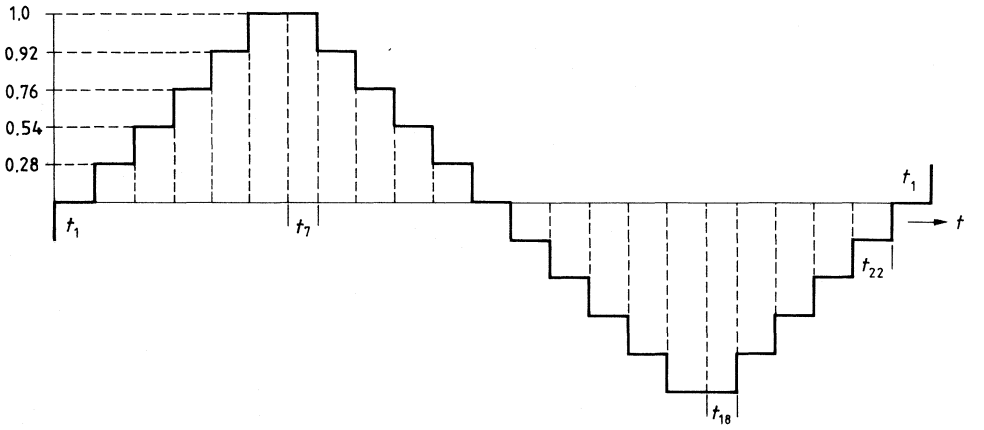


The thermal limitation (TL) overrides the quick charger (QC).

2. Tone generation

The on-chip oscillator generates together with the external clock crystal the master clock frequency f_{C1} = 4.194304 MHz. This master clock f_{C1} is scaled by a factor of 16 to f_{C2} = 262.144 kHz. The programmable dividers for the higher (f_5 ... f_8) and lower (f_1 ... f_4) frequency tone groups are driven by the clock f_{C2}. The programmable dividers generate the clock for the 6 bit *L/R* shift register. Each shift register controls one D/A converter and the polarity of its output waveform. The output sinewave is synthesized as a stairstep function with 11 voltage levels. The output waveform has 22 time segments (**fig. 3**). The time segments t_1 to t_6, t_8 to t_{17} and t_{19} to t_{22} are equal. The time segments t_7 and t_{18} are equal but slightly different from the others in order to meet the required output frequencies as closely as possible. The output waveforms are symmetrical; therefore, no even harmonics exist. The stairstep function with 11 voltage levels is calculated such that, theoretically, the lowest order harmonics are the 21st and the 23rd. Because of the different length of time segments t_7 and t_{18} and the tolerances of the D/A converter, lower odd harmonics exist.

Figure 3
Synthesized output waveforms



3. Output levels

Each D/A converter generates a five-level stairstep function. The mixer alternately reverses the polarity of the five-level stairstep function which leads to the symmetrical 11-level stairstep function (**fig. 3**). Furthermore, the mixer adds the stairstep function of the lower and of the higher frequency groups.

The nominal amplitudes of the stairstep function at the mixer output are:

Lower frequency group $i_{ML} = 42.5\ \mu A$
Higher frequency group $i_{MH} = 53.5\ \mu A$

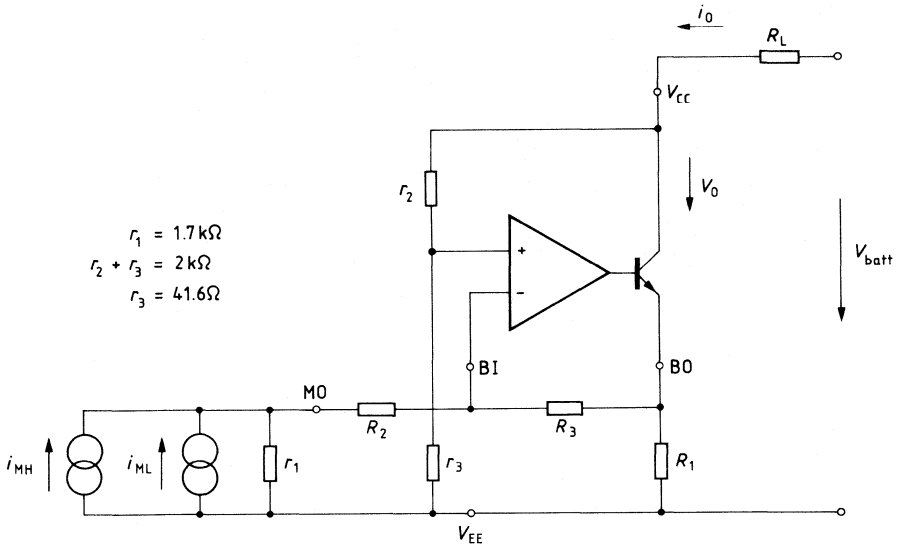
Figure 4 shows the AC-schematic of the output section of the PSB 8590. The feedback loop of the output amplifier is externally arranged. The resistors R_1 to R_3 determine the output level (V_{OL} and V_{OH}) and the output impedance R_O, as shown below.

$$R_O = \frac{R_1\,(r_2 + r_3)}{R_1 + r_3\left(1 + \dfrac{R_3 + R_1}{R_2 + r_1}\right)}$$

$$V_{OL,H} = i_{ML,\,H} \times \frac{(R_3 + R_1)\,R_L \times r_1}{R_1\,(R_2 + r_1)} \times \frac{R_O}{R_O + R_L}$$

The ratio of the resistors R_3/R_2 is restricted to the range $R_3/R_2 < 1.2$, otherwise the output amplitudes are clipped. Normally, the resistors R_2 and R_3 are equal. **Figure 8** shows the sum level P_S and the output impedance R_O as a function of R_1 and R_2.

Figure 4
AC schematic of the output stage



An external *RC* filter network is necessary in order to meet the CEPT recommendation concerning distortion and harmonics. The *RC* filter is easy to implement, because the pins MO, BI, BO, of the output amplifier are accessible. The PSB 8590 is shown in **figure 5** with a one-pole *RC* filter for application corresponding to the recommendations of the DBP and in **figure 6** with a two-pole *RC* filter for CEPT applications. **Figure 7** shows the output spectrum for the most critical case, the frequency f_8.

The nominal output levels $P_{L,H}$ are identical for the arrangement in **figure 5** and **figure 6**, they are

$$P_L = 20 \log \frac{V_{OL}}{\sqrt{2}\ \sqrt{1\ \text{mW} \times 600\ \Omega}} = -8.12\ \text{dBm}$$

$$P_H = 20 \log \frac{V_{OH}}{\sqrt{2}\ \sqrt{1\ \text{mW} \times 600\ \Omega}} = -6.12\ \text{dBm}$$

The sum output level P_S is

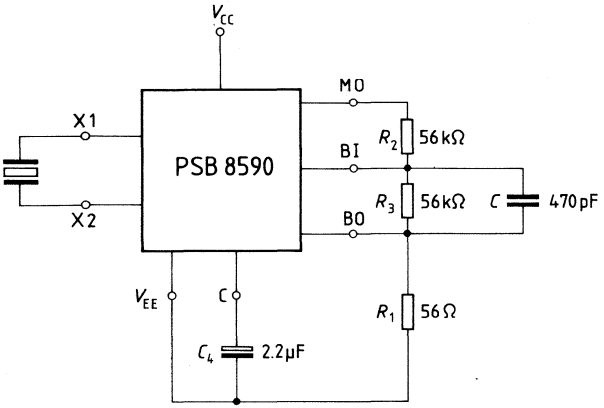
$P_S = 10 \log (10\ P_L/10 + 10\ P_M/10) = -4.0$ dBm

and the preemphasis P_D is

$P_D = P_H - P_L = 2$ dB

Figure 5

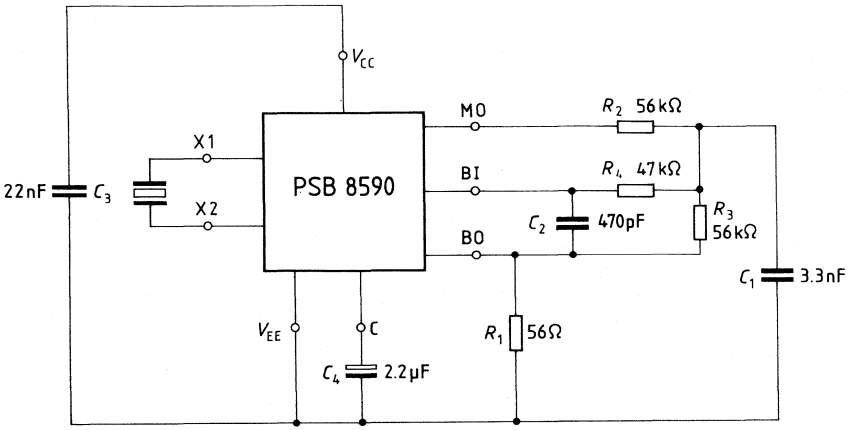
PSB 8590 with a 1-pole *RC* filter



In order to keep the insertion loss for all the DTMF frequencies less than 0.2 dB the 3 dB cutoff frequency of the filter should be at least 6 kHz.

Figure 6

PSB 8590 with a 2-pole *RC* filter (Butterworth)



The pole is $f_P \approx 2.7$ kHz

Figure 7

Output spectrum for frequency f_8 with a 2-pole Butterworth filter

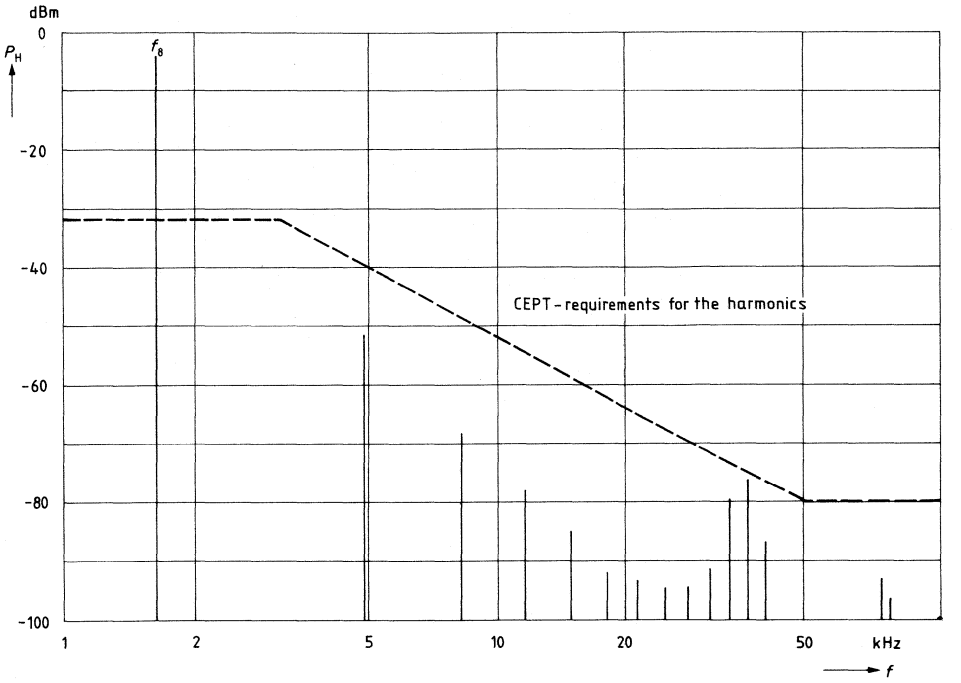
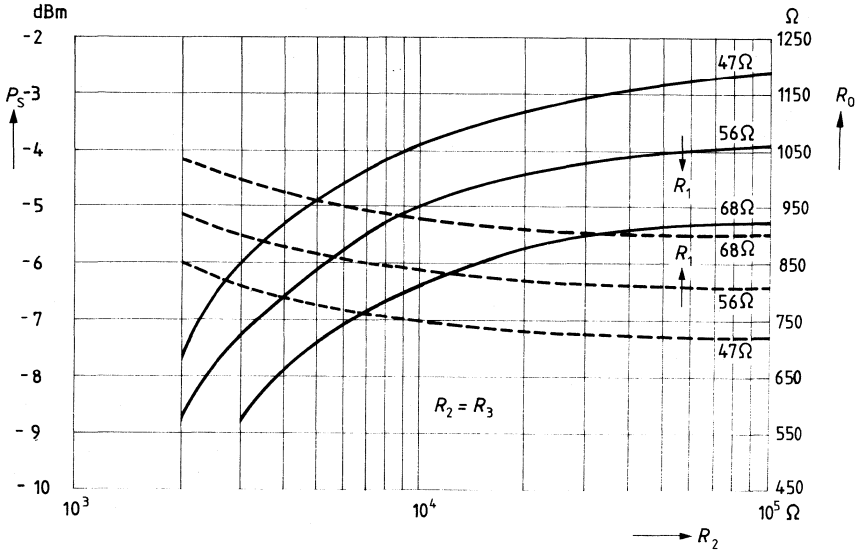


Figure 8

Sum output level P_S (–) and output impedance R_O (– – –) versus resistors R_1, R_2



4. Interface to keypad

There are three different operation modes of the interface:

a) Single contact 2–of–8 keypad
b) Electronic interface with a 2–of–8 keypad code
c) Electronic interface with a BCD code

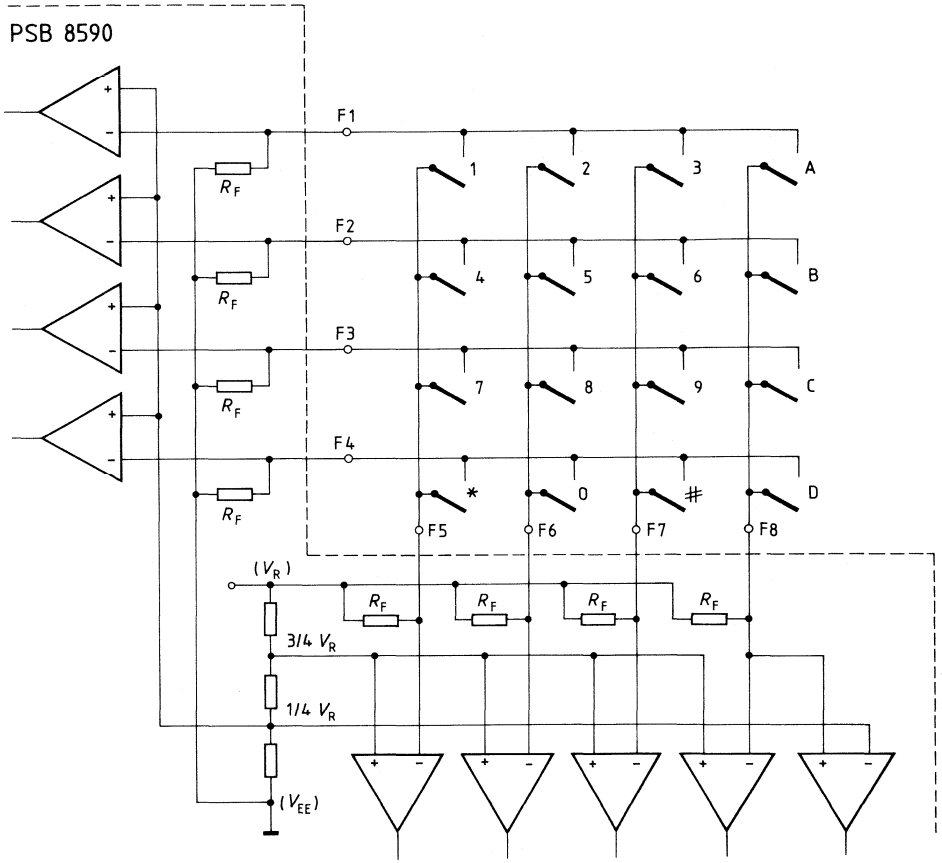
Figure 9 shows the schematic of the interface inputs F1 – F8. The inputs are divided into two groups F1 – F4 and F5 – F8. In addition, the pin F8 controls the operation modes. The resistors R_F are optimized for the single-contact keypad mode.

a) Interface to single contact or 2–of–8 keypads (**fig. 9**)

The buttons are debounced and electronically interlocked. If multiple buttons are pushed, the frequencies of the firstly activated button are generated. The requirements for the quality of the contacts are

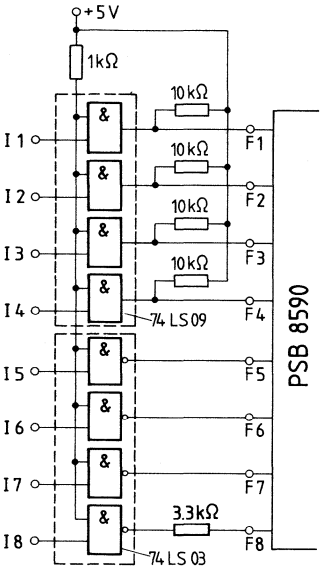
Contact open: OFF resistance $R_{OFF} > 50$ kΩ
Contact closed: ON resistance $R_{ON} \leqq 1$ kΩ
$I = 100$ μA

Figure 9
Schematic of keypad interface



b) Electronic interface with a 2–of–8 keypad code

Figure 10
Electronic control using the key code



The inputs I1 to I4 control the frequencies of the lower frequency group f_1 – f_4 and the inputs I5 to I8 control the frequencies of the higher frequency group. For the generation of a dual tone, one input of I1 to I4 of the lower group and one input of I5 to I8 of the higher group must have an H-level.

If more than one input of the respective group has an H-level, this is recognized as a multiple button push and the frequencies of the firstly sensed H-levels are generated.

Truth table

I1	1	2	3	A	Digit
I2	4	5	6	B	
I3	7	8	9	C	
I4	*	0	#	D	
Inputs	I5	I6	I7	I8	

c) Electronic interface with a binary code
Electronic control using the binary code

Figure 11a

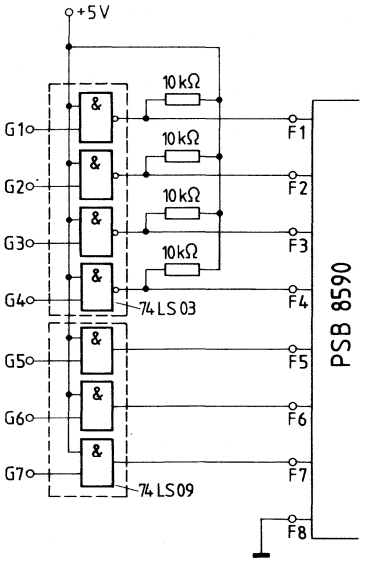


Figure 11b

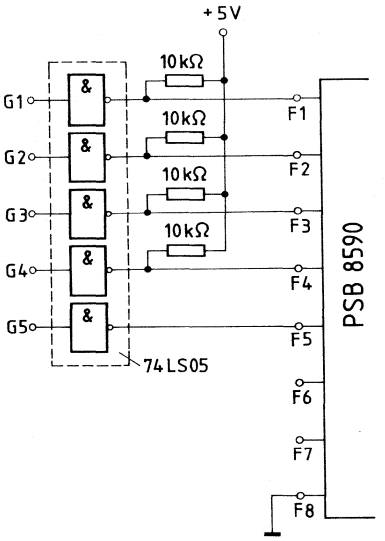


Figure 11a

This application enables both, dual and single frequency output.

The mode control input F8 is connected to ground. The dual tone pairs are generated corresponding to the binary code on the inputs G1 to G4. The enable inputs G5 to G7 have the following function:

G5 enable lower and higher frequency group; G6 enable higher frequency group F5 to F8; G7 enable lower frequency group F1 to F4

Figure 11b

This application is optimized for dual tone output without single tone capability.

G1 to G4 inputs for binary code; G5 enable lower and higher frequency group.

L-level enables the frequencies, H-level disables the frequencies. If the frequencies are disabled, the internal clock is inhibited.

Table information is present at inputs G1 to G4 in binary code

Digit	0	1	2	3	4	5	6	7	8	9	X	#	A	B	C	D
G4	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
G3	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
G2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
G1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H

Pin designation

Pin No.	Symbol	Description
1	V_{EE}	Negative line connection
2	MO	Mixer output
3	F1	Keyboard interface
4	F2	
5	F3	
6	F4	
7	BI	Input of output amplifier
8	BO	Output of output amplifier
9	X1	Connections for crystal $f = 4.194304$ MHz (2^{22} Hz)
10	X2	
11	F8	Keyboard interface and mode select
12	F7	Keyboard interface
13	F6	
14	F5	
15	C	Connection for filtering capacitor for the current sink
16	V_{CC}	Positive line connection

Electrical characteristics

Maximum ratings

		Min.	Max.	Unit
Voltage at any pin		V_{EE} −0.3 V	$V_{CC} - V_{EE}$	
Supply voltage	$V_{CC} - V_{EE}$	−0.3	14	V
Storage temperature	T_{stg}	−55	125	°C

Operating characteristics (T_{amb} = −25°C to 70°C)

		Test condition	Min.	Typ.	Max.	Unit
Supply current	I_S		16		120	mA
DC output voltage	V_S	16 mA < I_S < 120 mA	4.5	5	6	V
Internal reference voltage	V_R		1.15	1.25	1.35	V
Input resistors	R_F		2.5	3.5	4.5	kΩ
Input levels:						
Logical L	F1 – F4				0.15	V
Logical H	F1 – F4		0.5			V
Logical L	F5 – F7				0.7	V
Logical H	F5 – F8		1.1			V
Logical L	F8		0.5		0.7	V
BCD mode enable	F8				0.1	V

Operating characteristics (T_{amb} = −25°C to 70°C)

		Test conditions	Min.	Typ.	Max.	Unit
Output levels:						
Low group	P_L			−8.12		dBm
High group	P_H			−6.12		dBm
Sum level	P_S	I_S = 17 mA to 120 mA Fig. 12	−5.4	−4	−2.8	dBm
Preemphasis	P_D	I_S = 17 mA to 120 mA	1.8	2.4	2.8	dB
Sum level (frequencies disabled)	P_{SO}			−80		dBm
Output dynamic impedance	R_{DO}	I_S = 120 mA	600		1000	Ω
		I_S = 20 mA	660		1000	Ω
Timing specification:						
Tone frequency deviation	$\Delta f/f$		−2.9		+3.9	‰
Key debounce time	t_d		2		6	ms
Setup time (**fig. 13**)	t_S	I_S = 17 mA to 20 mA			7	ms
		I_S = 20 mA to 120 mA			5	ms

Tone frequency deviation (without tolerances of crystal)

	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	Unit
Required frequency	697	770	852	941	1209	1336	1477	1633	Hz
Generated frequency*)	697.2	771.0	851.1	943	1212.6	1337.5	1472.7	1638.4	Hz
Deviation	2.75	1.374	−1.037	2.087	3.829	1.1	−2.898	3.307	‰

*) The generated frequencies are derived from a clock crystal with 4.194304 MHz (2^{22} Hz).

Figure 12

Measuring circuit for outputs sum level P_{SO}

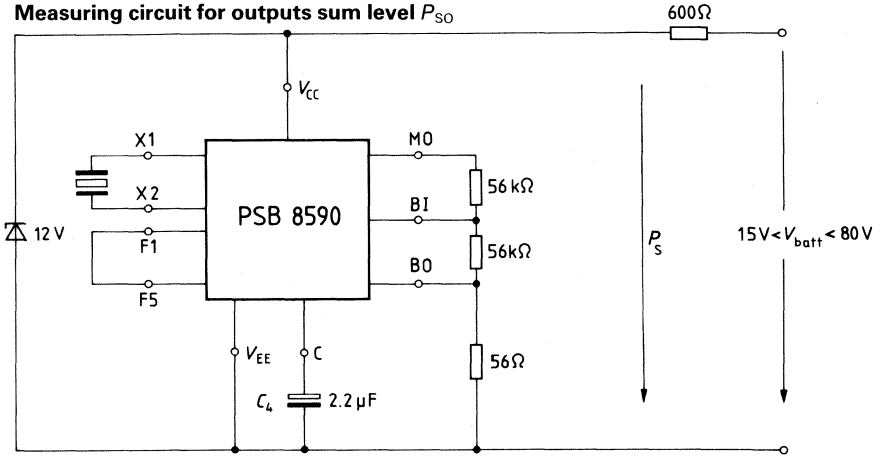


Figure 13
Circuit for measuring setup time t_S

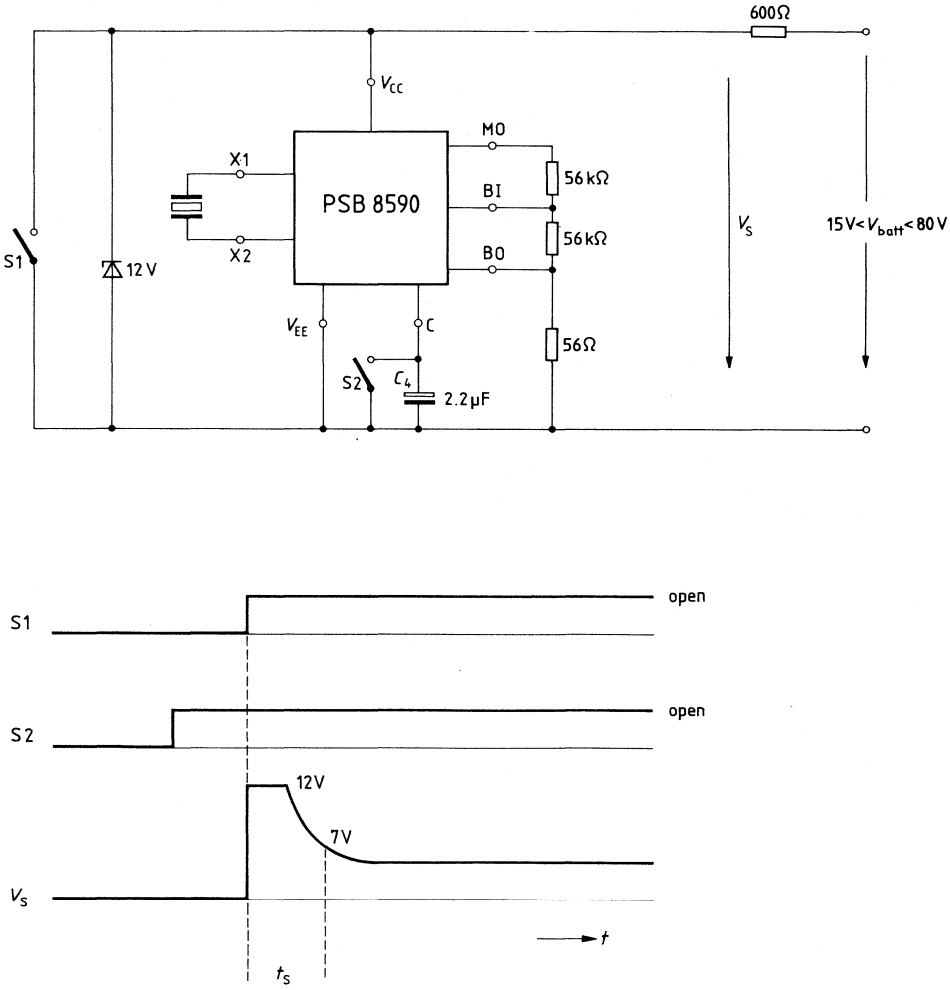
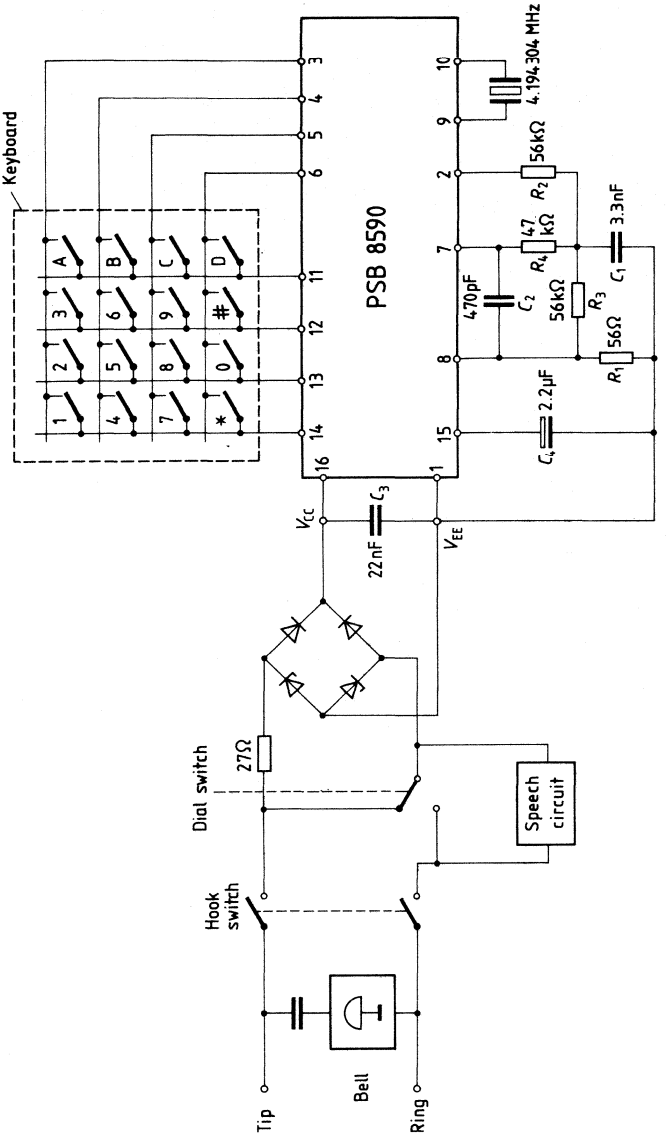


Figure 14

Typical telephone application of the PSB 8590 with 2-pole *RC* filter (Butterworth) for CEPT recommendations



Telephone Controller (Single-Chip 8 Bit CMOS Microcomputer)

SAB 80C482 (SM 850)

Preliminary data

MOS circuit

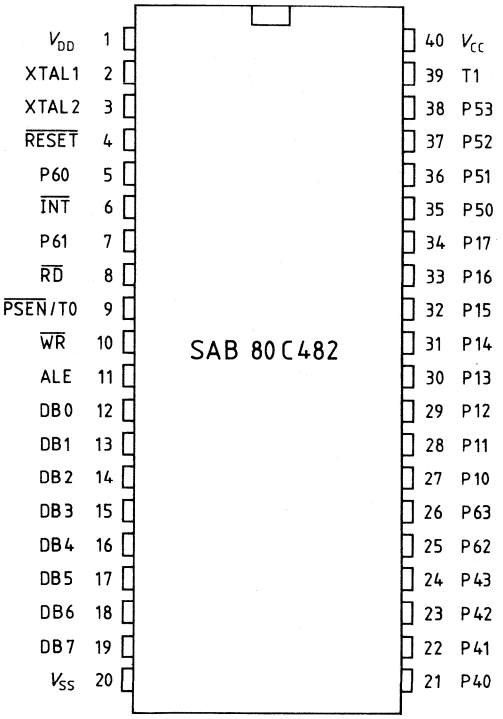
Type	Ordering code	Package outline
SAB 80C482	Q67100-Z154	DIP 40

Siemens SAB 80C482 is a low power, advanced CMOS member of the popular SAB 8048 family. The CMOS design of the SAB 80C482 opens new application areas that require battery operation, low power standby, wide voltage range and the ability to maintain operation during AC power line interruption. These application include portable and hand-held instruments, telecommunications, consumer and automotive.

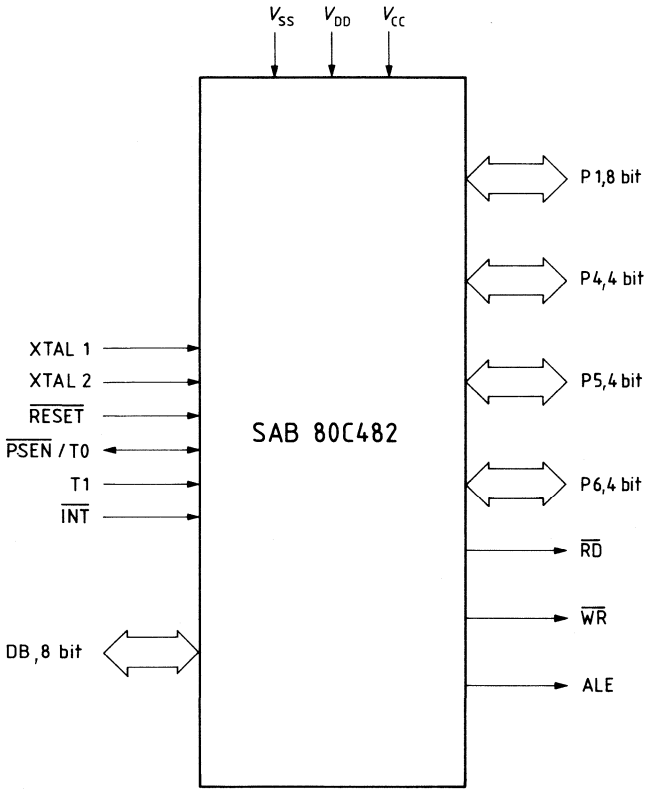
The SAB 80C482 supports these applications with new additional features, like 4 I/O lines more than in the SAB 8048, automatic keyboard scanning, idle mode and power-on reset. This specification mainly describes the differences between the SAB 80C482 and SAB 8048. For detailed SAB 8048 information see the SAB 8048 user manual.

- Member of SAB 8048 family
- 8 bit CPU, ROM, RAM, I/O in single package
- Supply voltage 2.5 to 6 V
- Fully static microcomputer; clock 0 to 3 MHz
- 2K × 8 ROM
  64 × 8 RAM
  31 I/O lines
- Power on reset
- Two power consumption
  Normal operation: 1mA, 1MHz, 5V
  Standby mode: 15 µA, 5V
- Keyboard scanning function
- 90 instructions
- 2.66 µs cycle with 3 MHz XTAL all instructions 1 or 2 cycles

Pin configuration
top view



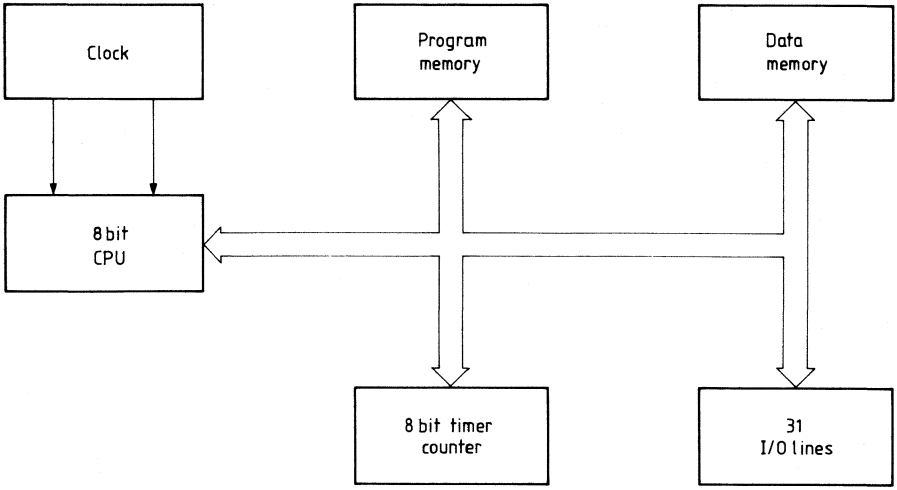
Logic symbol



Pin designation

Pin No.	Symbol	Description
2	XTAL1	Oscillator input; one side of crystal input
3	XTAL2	Oscillator output; other side of crystal input
4	$\overline{\text{RESET}}$	Input which is used to initialize the processor (active low)
6	$\overline{\text{INT}}$	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after reset. In the idle mode the interrupt terminates idle when interrupt is enabled (active low)
8	$\overline{\text{RD}}$	Output strobe activated during a bus read. Can be used to enable transfer of data onto the BUS from an external device. Used as a read to external data memory (active low)
9	$\overline{\text{PSEN}}$/T0	Program store enable. This output occurs only during a fetch to external program memory (active low). In system without ROM expansion pin 9 is testable using the JT0 and JNT0 instructions. Execution of SEL MB instruction defines the pin as an output pin for external ROM access program store enable until reset occurs
10	$\overline{\text{WR}}$	Output strobe during a BUS write. Used as write strobe to external data memory. Used as input to activate the continuous reading of internal ROM without ROM execution (active low)
11	ALE	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory
12...19	DB0...DB7	True bidirectional port which can be written or read synchronously using $\overline{\text{WR}}$, $\overline{\text{RD}}$ strobes
21...24	P40...P43	4 bit quasi-bidirectional port. Internal pullup. Additional port for program counter bit 8...11 if external ROM is selected
5, 7, 25, 26	P60...P63	4 bit quasi-bidirectional port. Internal pullup. Mask-programmable for additional keyboard scanning function
27...34	P10...P17	8 bit quasi-bidirectional port. Internal pullup. Mask-programmable for additional keyboard scanning function
35...38	P50...P53	4 bit quasi-bidirectional port. Internal pullup. Mask-programmable for additional keyboard scanning function
39	T1	Input pin testable using the JT1 and JNT1 instructions. Can be designated as timer/counter input using the STRT CNT instruction
40	V_{CC}	Main power supply for all functional blocks not noticed for pin 1
1	V_{DD}	Power supply for RAM, PC and SP
20	V_{SS}	Circuit GND potential (0V)

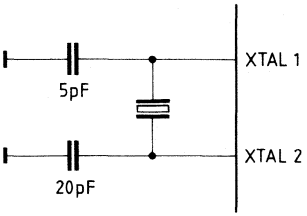
Block diagram



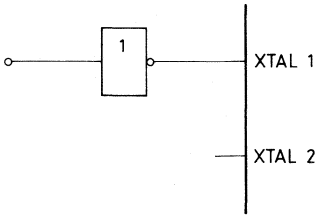
Oscillator

The on-board oscillator is a high gain resonant circuit with a frequency range of 0 to 3 MHz. Clock frequency depends on resonator (e.g. quartz) connected between pin XTAL1 and XTAL2.

Crystal oscillator mode



Driving from external source



8 bit timer/counter

The SAB 80C482 contains a timer/counter to aid the user in counting external events and generating accurate time delays without placing a burden on the processor for these functions.

Timer

Execution of a START T instruction connects an internal clock to the counter input. The XTAL frequency divided by 256 is the timer input frequency.

Counter

Execution of a START CNT instruction connects the T1 pin to the counter input and enables the counter. Subsequent high to low transition on T1 pin must be held low for at least one machine cycle to insure it won't be missed. The maximum rate at which the counter may be incremented is once per three instruction cycles. There is no minimum frequency limit.

Program memory

Resident program memory consists of 2048 bytes. There are three locations in program memory of special importance:

1. **Location 0:** Executing the initialization reset causes the first instruction to be fetched from location 0.
2. **Location 3:** Execution starts at location 3 after the interrupt input line (pin 6) of the processor is low (if interrupt is enabled).
3. **Location 7:** A timer/counter interrupt resulting from timer/counter overflow (if enabled).

Four different operation modes of processor program memory configurations are possible:

1. Internal 2Kbytes ROM

- Pin 9 is available as T0 input
- P40...P43 is an I/O port without restrictions.

2. Internal 2Kbyte ROM and additional external 2Kbytes

- The first instruction (PC = 0) must be an SEL MB0/1 instruction to select the $\overline{\text{PSEN}}$ output mode for pin 9.
- Execution of SEL MB instruction and next execution of a CALL or JMP instruction enables external ROM access.
- To access the external 2K of program memory, a select memory bank (SEL MB1) and a JMP or CALL instruction must be executed to exceed the 2K boundary.
- Access to external ROM will cause the program counter bits 8...11 to be issued at P40...P43.
- Executing an MOVP3 A, @A instruction the internal ROM will be selected.
- Executing an interrupt CALL subroutine the internal ROM will be selected till the subroutine is finished with an RETR instruction.
- In the 2nd cycle of MOVX instructions no $\overline{\text{PSEN}}$ signal will occur, the ALE will be active.

3. External 4Kbyte ROM, internal ROM is disabled

- Access to external 4Kbyte ROM and disabled internal ROM can be achieved by a low pulse to pin 8 during the reset.
- Pin 9 is selected as $\overline{\text{PSEN}}$ output.
- Program counter bits 0...7 will be issued at DB0...DB7, bit 8...11 will be issued at P40...P43.
- ALE is activated.
- Execution of MOVP3 A, @A instruction or an interrupt service subroutine enables the lower 2Kbyte external ROM.

4. Test operation for continuous reading of the internal ROM without program execution

- Connecting pin 10 with V_{SS} in the period of ALE will cause a test operation with continuous reading of the internal ROM without program execution.
- The content of internal ROM will be issued via DB0...DB7 to check resident program.
- Program counter bit 0...7 will be issued at DB0...DB7 and bit 8...11 will be issued at P40...P43.
- ALE and $\overline{\text{PSEN}}$ are enabled.

Interrupt

Three different interrupts are possible:

1. External interrupt by applying a low level input to the $\overline{INT}$ pin.
2. Timer/counter interrupt. When the counter increments from maximum count (FF) to zero an overflow occurs.
3. By pulling down (V_{SS}) one of the port pins P1, P5 or P6 when these are mask-programmed and the processor is in HALT state. In this case, the next instruction after HALT will be executed.

Reset

The reset input provides a means for initialization of the processor.
Reset performs the following functions:

1. Sets program counter to zero
2. Sets stack pointer to zero
3. Selects register bank 0
4. Selects memory bank 0
5. Sets BUS to high impedance state
6. Sets BUS latches to low state
7. Sets port 1, 4, 5 and 6 to input mode
8. Sets port latches 1, 4, 5 and 6 to high state
9. Disables interrupts (timer and external)
10. Stops timer
11. Clears timer flag
12. Sets HALT mode released

The following conditions should be noticed:

1. Reset signal does not affect the RAM.
2. Powering all functional blocks while the reset pin 4 is pulled to ground (V_{SS} pin 20) will cause the reset condition for all functional blocks.
3. Pulling down reset pin 4 to ground releases the HALT mode. The program starts with PC = 0.
4. The moment of the first instruction cycle (PC = 0) after the initialization reset depends on following factors:
   a) Rise time of power supply
   b) Build-up period of oscillator which itself depends on the quality of the resonator
   c) Synchronization time of pulse generator
   d) Period length of reset pulse

5. An additional feature of SAB 80C482 is the power-on reset capability for raising V_{CC} and/or V_{DD}.
6. Following operation modes are possible:
   a) One power supply. Initialization reset by power-on reset.
      No standby operation (**fig. A**)
   b) One power supply. Initialization reset by pin 4.
      No standby operation (**fig. B**)
   c) Two power supplies. Initialization reset by power-on reset.
      Power-on reset when leaving the standby operation (**fig. C**)
   d) Two power supplies. Initialization reset by pin 4 (**see fig. B**).
      Standby operation introduced by an HALT instruction.
      Power-on reset when leaving the standby operation (**see fig. D**)
   e) Two power supplies. Initialization reset and when leaving the standby operation by reset pin 4 (**see fig. E**).

   Saved data for operation mode **figure C** and **D** if the HALT mode has been released by an interrupt: RAM, PC 0 = 11, SP (Special keyboard function can't be used because data bus is in high impedance mode after executing standby reset). Saved data for operation in mode **figure E:** RAM.

Figure A

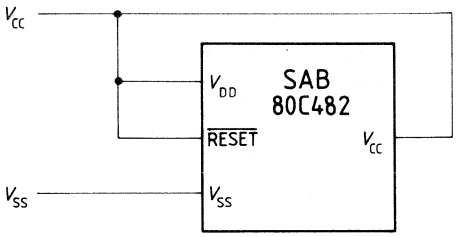


Figure B

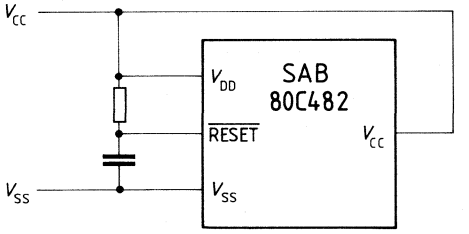


Figure C

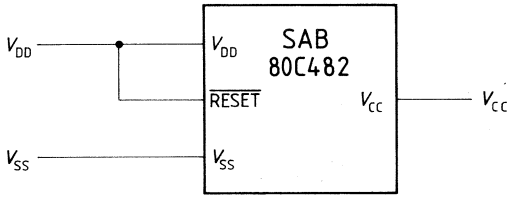


Figure D

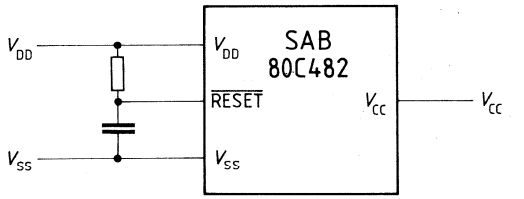
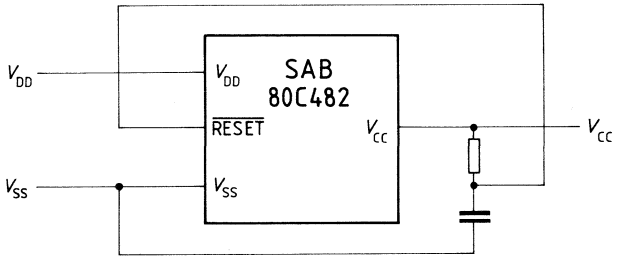


Figure E



HALT state

After the execution of the HALT instruction the processor will be in the HALT state. In the HALT state, I_{CC} and I_{DD} current is about 400 µA.
The oscillator will be running.
The release of HALT operation is possible in three different ways:

1. By low pulse to the $\overline{\text{RESET}}$ pin (PC = 0)
2. By low pulse to a ROM mask-programmed port pin (PC) + 1 = >(PC).
3. By low pulse to the $\overline{\text{INT}}$ pin.
   - If the interrupt is disabled, the processor will continue with the next instruction after the HALT instruction (PC) + 1 = > (PC).
   - If interrupt is enabled, the processor will continue with an interrupt CALL subroutine 003 = > (PC).

Structogram for a keyboard scanning example:

high to PORT low to BUS HALT instruction	(output Y information) (input X information)
wait until pushbutton interrupt	
high to BUS high to PORT 8 to cycle counter complement bit 0 of BUS and set BUS with this information	
repeat until cycle counter = 0	
read PORT and store	
high to BUS high to PORT shift left BUS information decrement cycle counter	
compute pushbutton address	

Keyboard controller

For special applications the following ports can be used as additional hardware interrupt inputs (without execution of an interrupt call-subroutine, software priority levels are possible):

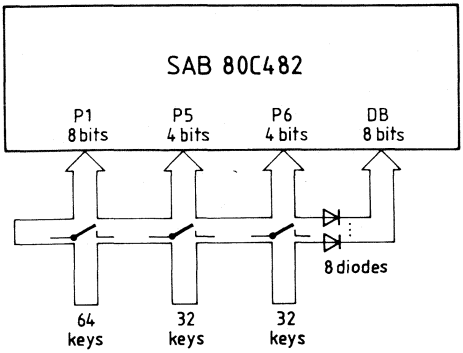
	Port 1 (lower and/or higher nibble)
AND/OR	Port 5
AND/OR	Port 6

The four internal mask-programmable NAND gates can be connected to the port pins by ROM mask-programming.

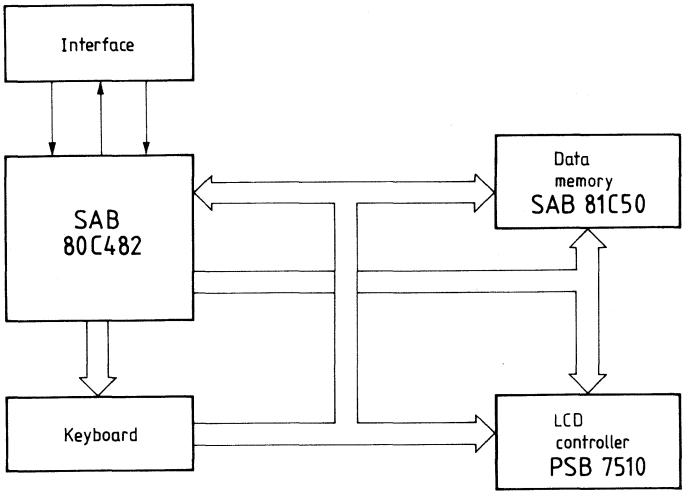
By pulling down to V_{SS} one of these programmed port pins while the processor is in the HALT state, the HALT state is released and the processor will start operating with the program after the HALT instruction.

Not programmed port pins can be used as normal I/O ports.

Example for maximal configuration



Application example "Special Features Telephone Set"



Function features (example)

- Stack for direct and indirect redialing
- Short dialing
- Auto dialing by special keys
- Babysitter function
- LC – display control
- Electronic keylock
- Clock function
- Rate signaling
- Interrupt of internal telephone connections

Instruction set

The software differences between SAB 8048/49 and SAB 80C482

There are 5 new instructions, additionally to the SAB 8048 instruction set:

DEC	@R0	instruction code	C0
DEC	@R1	"	" C1
DJNZ	@R0, addr	"	" E0
DJNZ	@R1, addr	"	" E1
HALT		"	" F3

The following SAB 8048 instructions are not available:

IN	A, P2	Instruction code	0A
MOVD	A, P7	"	" 0F
OUTL	P2, A	"	" 3A
MOVD	P7, A	"	" 3F
ENT0	CLK	"	" 75
JF1	addr	"	" 76
CLR	F0	"	" 85
ORL	P2, #data	"	" 8A
ORLD	P7, A	"	" 8F
CPL	F1	"	" 95
ANL	P2, #data	"	" 9A
ANLD	P7, A	"	" 9F
CLR	F1	"	" A5
CPL	F1	"	" B5
JF0	addr	"	" B6
MOV	A, PSW	"	" C7
MOV	PSW, A	"	" D7
JNI	addr	instruction code	66 (8048 = 86)

Symbols and abbreviations

A, Accu	Accumulator
AC	Auxiliary carry
addr	Program memory address
An	Accumulator bit n
BUS	Bus-Port
CY	Carry
data	Constant (8 bit)
DBF	Memory bank flipflop
INT\	External interrupt input
PC	Program counter
Pp	Port 4...6
P1	Port 1
PSW	Program status word
Ri	Register 0, 1
Rr	Register 0...7
SP	Stack pointer
T	Timer/counter
TF	Timer flag
T0, T1	Inputs T0, T1
X	External data memory 8 bit
#	Immediate data prefix
@	Indirect address prefix
Page	Programm memory block (256 byte)
( )	Content
→	Is transferred to
⟷	Is exchanged with
AND	Logical AND
OR	Logical OR
XOR	Logical EXCLUSIV-OR
\	Negation
<>	Not equal

Mnemonic	Function	Description	HEX-Code	Flag	Bytes	Cycles
Accumulator and register move instructions						
MOV A, Rr	(Rr) → A	Move register to Accu	F8-FF		1	1
MOV A, @Ri	((Ri)) → A	Move data memory to Accu	F0-F1		1	1
MOV A,#data	data → A	Move immediate data to Accu	23		2	2
MOV Rr,A	(A) → Rr	Move Accu to register	A8-AF		1	1
MOV @Ri,A	(A) → (Ri)	Move Accu to data memory	A0-A1		1	1
MOV Rr,#data	data → Rr	Move immediate data to register	B8-BF		2	2
MOV @Ri, #data	data → (Ri)	Move immediate data to data memory	B0-B1		2	2
MOVX A,@Ri	((Ri)) → A	Move external data memory to Accu	80-81		1	2
MOVX @Ri,A	(A) → (Ri)	Move Accu to external data memory	90-91		1	2
XCH A,Rr	(Rr) ⟷ (A)	Exchange Accu and register	28-2F		1	1
XCH A,@Ri	((Ri)) ⟷ (A)	Exchange Accu and data memory	20-21		1	1
XCHD A,@Ri	((Ri)) 0-4 ⟷ (A) 0-4	Exchange nibble of Accu and data memory	30-31		1	1
MOVP3 A,@A	save (PC) (A) → PC0-7 011 → PC8-11 ((PC)) → A restore PC	Move data of program memory page 3 to Accu	E3		1	2
MOVP A,@A	save (PV) (A) → PC0–7 ((PC)) → A restore PC	Move data of program memory current page to Accu	A3		1	2
SWAP A	(A) 0-3 ⟷ (A) 4-7	Swap nibbles of Accu	47		1	1
Timer/counter move instructions						
MOV A,T	(T) → A	Read timer/counter to Accu	42		1	1
MOV T,A	(A) → T	Load timer/counter from Accu	62		1	1
Port move instructions						
IN A,P1	(P1) →A	Input port 1 to Accu	09		1	2
OUTL P1,A	(A) → P1	Output Accu to port 1	39		1	2
ANL P1,#data	(P1) AND data → P1	AND immediate data to port 1	99		2	2
ORL P1,#data	(P1) OR data → P1	OR immediate data to port 1	89		2	2
INS A,BUS	(BUS) → A	Input BUS to Accu	08		1	2
OUTL BUS,A	(A) → BUS	Output Accu to BUS	02		1	2
ANL BUS, #data	(BUS) AND data → BUS	AND immediate data to BUS	98		2	2
ORL BUS, #data	(BUS) OR data → BUS	OR immediate data to BUS	88		2	2

Mnemonic	Function	Description	HEX-Code	Flag	Bytes	Cycles
MOVD A,Pp	(Pp) → A0-3 0 → A4-7	Input port 4-6 to Accu	OC-OE		1	2
MOVD Pp,A	(A) 0-3 → Pp	Output Accu to port 4-6	3C-3E		1	2
ANLD Pp,A	(A) 0-3 and (Pp) → Pp	AND Accu to port 4-6	9C-9E		1	2
ORLD Pp,A	(A) 0-3 OR (Pp) → Pp	OR Accu to port 4-6	8C-8E		1	2
Arithmetic instructions with accumulator						
ADD A,Rr	(A)+(Rr) → A	Add register to Accu	68-6F	AC CY	1	1
ADD A,@Ri	(A)+((Ri)) →A	Add data memory to Accu	60-61	AC CY	1	1
ADD A,#data	(A)+data → A	Add immediate data to Accu	03	AC CY	2	2
ADDC A, Rr	(A)+(Rr)+(CY) → A	Add register with carry to Accu	78-7F	AC CY	1	1
ADDC A, @Ri	(A)+((Ri))+ (CY) → A	Add data memory with carry to Accu	70-71	AC CY	1	1
ADDC A,#data	(A)+(data)+ (CY) → A	Add immediate data with carry to Accu	13	AC CY	2	2
INC A	(A)+1 → A	Increment Accu	17		1	1
DEC A	(A)−1 → A	Decrement Accu	07		1	1
DA A		Decimal adjust Accu	57	AC CY	1	1
Arithmetic instructions with registers						
INC Rr	(Rr)+1 → Rr	Increment register	18-1F		1	1
DEC Rr	(Rr)−1 → Rr	Decrement register	C8-CF		1	1
INC @Ri	((Ri))+1 → (Ri)	Increment data memory	10-11		1	1
DEC @Ri	((Ri))−1 → (Ri)	Decrement data memory	C0-C1		1	1
DJNZ Rr,addr	(Rr)−1 → Rr if (Rr) <> 0 addr → PC0-7	Decrement register and jump if not zero	E8-EF		2	2
DJNZ @Ri,addr	((Ri))−1 → Ri if ((Ri)) <> 0 addr → PC0-7	Decrement data memory and jump if not zero	E0-E1		2	2
Logical instructions with accumulator and registers						
ANL A,Rr	(A) AND (Rr) → A	AND register to Accu	58-5F		1	1
ANL A,@Ri	(A) AND ((Ri)) → A	AND data memory to Accu	50-51		1	1
ANL A,#data	(A) AND data → A	AND immediate data to Accu	53		2	2
ORL A,Rr	(A) OR (Rr) → A	OR register to Accu	48-4F		1	1

Mnemonic	Function	Description	HEX-Code	Flag	Bytes	Cycles
ORL A,@Ri	(A) OR ((Ri)) → A	OR data memory to Accu	40-41		1	1
ORL A,#data	(A) OR data → A	OR immediate data to Accu	43		2	2
XRL A,Rr	(A) XOR (Rr) → A	XOR register to Accu	D8-DF		1	1
XRL A,@Ri	(A) XOR ((Ri)) → A	XOR data memory to Accu	D0-D1		1	1
XRL A,#data	(A) XOR data → A	XOR immediate data to Accu	D3		2	2
CLR A	0 → A	Clear Accu	27		1	1
CPL A	(A) \ → A	Complement Accu	37		1	1
Rotate instructions						
RL A	(An) → An+1	Rotate Accu left	E7		1	1
RCL A	(An) → An+1 (A7) → CY (CY) → A0	Rotate Accu left through carry	F7	CY	1	1
RR A	(An+1) → An	Rotate Accu right	77		1	1
RRC A	(An+1) → An (A0) → CY (CY) → A7	Rotate Accu right through carry	67	CY	1	1
Flag instructions						
CLR C	0 → CY	Clear carry	97	CY	1	1
CPL C	(CY) \ → CY	Complement carry	A7	CY	1	1
Branch instructions						
JMP add	addr0-7 → PC0-7 addr8-10 → PC8-10 DBF → PC11	Jump unconditional page 0 1 2 3 4 5 6 7	04 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
JMPP @A	((A)) → PC0-7	Jump to address defined in program memory	B3		1	2
JC addr	if (CY) = 1 addr → PC0-7	Jump if carry = 1	F6		2	2
JNC addr	if (CY) = 0 addr → PC0-7	Jump if carry = 0	E6		2	2
JZ addr	if (A) = 0 addr → PC0-7	Jump if Accu = 0	C6		2	2
JNZ addr	if (A) <> 0 addr → PC0-7	Jump if Accu <> 0	96		2	2
JT0 addr	if T0 = 1 addr → PC0-7	Jump if input T0 = 1	36		2	2
JNT0 addr	if T0 = 0 addr → PC0-7	Jump if input T0 = 0	26		2	2

Mnemonic	Function	Description		HEX-Code	Flag	Bytes	Cycles
JT1 addr	if T1 = 1 addr → PC0-7	Jump if input T1 = 1		56		2	2
JNT1 addr	if T1 = 0 addr → PC0-7	Jump if input T1 = 0		46		2	2
JTF addr	if TF = 1 addr → PC0-7 0 → TF	Jump if timer flag = 1		16	TF	2	2
JNI addr	if INT\ = 0 addr → PC0-7	Jump if input INT\ = 0		66		2	2
JBN addr	if (An) = 1 addr → PC0-7	Jump if Accu bit n = 1	n = 0 1 2 3 4 5 6 7	12 32 52 72 92 B2 D2 F2		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
Subroutine instructions							
CALL addr	(PC0-7,PSW4-7) → (SP) (SP)+1 → SP addr0-7 → PC0-7 addr8-10 → PC0-10 DBF = PC11	Jump to subroutine	page 0 1 2 3 5 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
RET	(SP)−1 → SP ((SP)) → PC	Return from subroutine		83		1	2
RETR	(SP)−1 → SP ((SP)) → PC ((SP)) → PSW4-7	Return from subroutine and restore		93		1	2
Control instructions							
STRT T		Start timer		55		1	1
STRT CNT		Start counter		45		1	1
STOP TCNT		Stop timer/counter		65		1	1
EN TCNTI		Enable timer/counter interrupt		25		1	1
DIS TCNTI		Disable timer/counter interrupt		35		1	1
EN I		Enable external interrupt		05		1	1
DIS I		Disable external interrupt		15		1	1
SEL RB0		Select register bank 0		C5		1	1
SEL RB1		Select register bank 1		D5		1	1
SEL MB0		Select memory bank 0 Select pin 9 as $\overline{\text{PSEN}}$ output		E5		1	1
SEL MB1		Select memory bank 1 Select pin 9 as $\overline{\text{PSEN}}$ output		F5		1	1
NOP		No operation		00		1	1
HALT		HALT instruction		F3		1	1

Maximum ratings

Ambient temperature under bias	T_{amb}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Voltage at any pin with respect to GND (V_{SS})	V	0 to 7	V
Total power dissipation	P_{tot}	1	W

DC characteristics

T_{amb} = 0 to 70°C; V_{CC} = 2.5 to 6 V; V_{SS} = 0 V

		Test conditions	Min.	Typ.	Max.	Unit
L input voltage (all except XTAL1, XTAL2)	V_{IL}		−0.1		0.2	V
L input voltage (XTAL1, XTAL2)	V_{IL}		−0.1		0.15	V
H input voltage (all except XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IH}		0.7		V_{CC}	V
H input voltage $\overline{\text{RESET}}$, XTAL1, XTAL2	V_{IH1}		0.8		V_{CC}	V
L output voltage (BUS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	V_{OL}	I_{OL} = 1.0 mA			0.45	V
H output voltage (BUS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, ALE)	V_{OH}	I_{OH} = −100 µA				V
H output voltage (all other outputs)	V_{OH1}	I_{OH} = −1 µA				V
Input current (Port 1, 4, 5, 6)	I_{ILP}	$V_{IN} \leqq V_{IL}$			− 30	µA
Input current ($\overline{\text{RESET}}$)	I_{ILC}	$V_{IN} \leqq V_{IL}$			− 40	µA
Input leakage current (T1, $\overline{\text{INT}}$)	I_{IL}	$V_{SS} < V_{IN} < V_{CC}$			±10	µA
Output leakage current (BUS, T0) high impedance state	I_{CL}	$V_{SS} < V_{IN} < V_{CC}$			±10	µA
Total supply current	$I_{DD} + I_{CC}$	1 MHz			1.2	mA
HALT power supply current	I_{CC}	1 MHz			400	µA
Power down mode	I_{CC}				15	µA

AC characteristics

Read from, write to and instruction fetch from external data and program memory
T_{amb} = 0 to 70°C; V_{CC} = 5V; V_{SS} = 0V; f_{osc} = 3 MHz

		Test conditions	Min.	Typ.	Max.	Unit
ALE pulse width	t_{LL}		833			ns
Address setup before ALE	t_{AL}		166			ns
Address hold from ALE	t_{LA}		0		200	ns
Control pulse width						
$\overline{PSEN}$	t_{CC}		333			ns
$\overline{RD}$, $\overline{WR}$	t_{CC}		1333			ns
Data setup before $\overline{WR}$	t_{DW}		1333			ns
Data hold after $\overline{WR}$	t_{WD}	t_{CY} = 2.66 µs C_{LC} = 20 pF	333			ns
Cycle time	t_{CY}		2.66			µs
Data hold	t_{DR}		0		200	ns
$\overline{RD}$ to data in	t_{RD}		1166			ns
$\overline{PSEN}$ to data in	t_{RD}		166			ns
Address setup before $\overline{WR}$	t_{AW}		1666			ns
Address setup before data in						
$\overline{RD}$	t_{AD}		3166			ns
$\overline{PSEN}$	t_{AD}		500			ns
Address float to						
$\overline{RD}$	t_{AFC}		166			ns
$\overline{PSEN}$	t_{AFC}		333			ns
Control pulse to ALE						
$\overline{WR}$	t_{CA}		0		200	ns
$\overline{RD}$	t_{CA}			333		ns
$\overline{PSEN}$	t_{CA}			1333		ns

Time parameters versus f_{osc}

	Parameter	Unit
t	$1/f_{osc}$	µs
t_{CY}	8t	µs

Read from external data memory

t_{LL}	2.5 t	µs
t_{CA}	–	ns
t_{AFC}	1.0 t	µs
t_{CC}	4.0 t	µs
t_{DR}	–	ns
t_{RD}	3.5 t	µs
t_{AD}	9.5 t	µs

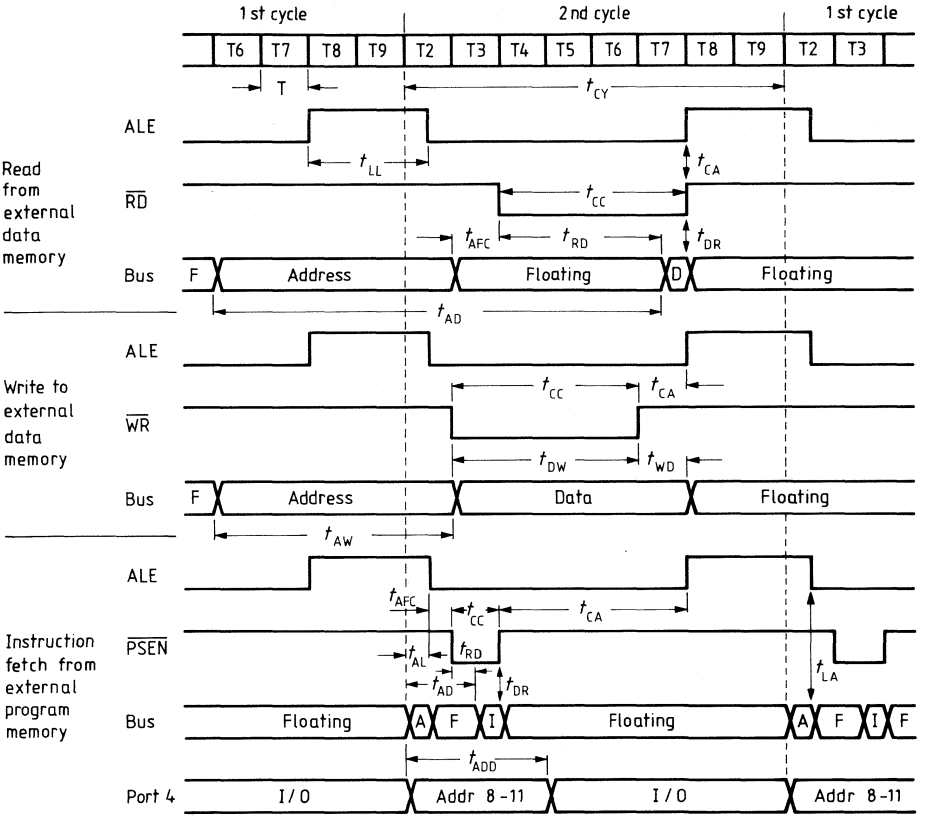
Write to external data memory

t_{CA}	1.0 t	µs
t_{CC}	4.0 t	µs
t_{WD}	1.0 t	µs
t_{DW}	4.0 t	µs
t_{AW}	5.0 t	µs

Instruction fetch from external program memory

t_{AL}	0.5 t	µs
t_{CA}	4.0 t	µs
t_{LA}	–	ns
t_{CC}	1.0 t	µs
t_{DR}	–	µs
t_{RD}	0.5 t	µs
t_{AD}	1.5 t	µs
t_{ADD}	3.0 t	µs
t_{AFC}	0.5 t	µs

Waveforms



A ... Address
D ... Data
F ... Floating
I ... Instruction

Advance information

MOS circuit

Type	Ordering code	Package outline
PSB 7510	see table	MICROPACK *) 64 connections

The PSB 7510 monolithic integrated circuit controls numeric LC-displays in quadruple multiple operation.

Due to "MICROPACK" outline (film carrier), the LC-display units are extremely thin and compact.

Features

- CMOS Si-gate technology
- Supply voltage 2.5 V to 6 V
- Display up to 20 digits, 7 segment
- MUX 4
- On-chip oscillator
- Cursor or blinking selectable
- Selection of one flag per digit available
- 2 different character sets
  (0 – 9, 3 bars, blank or
  0 – 9, 2 bars. A, b, c, d, blank)
- 64 pin MICROPACK

	Type	Ordering code	Quantity per order unit (piece)	Minimum shipping quantity (piece)	Maximum shipping quantity (piece)
Large quantities					
film	PSB 7510	Q67100-Z155	1500...2500	100	–
Samples					
punched out	PSB 7510	Q67100-Z155-E20	5	5	50
DIP 64 intermediate carrier	PSB 7510	Q67100-Z155-E21	1	1	5

For **prototyping,** limited quantities of components can be delivered as punched out MICROPACKs, or soldered on a DIP 64 intermediate carrier.

Shipment of **large quantities** will be on metal film spools (CMOS!).
These film spools are the property of Siemens and must be returned when empty.

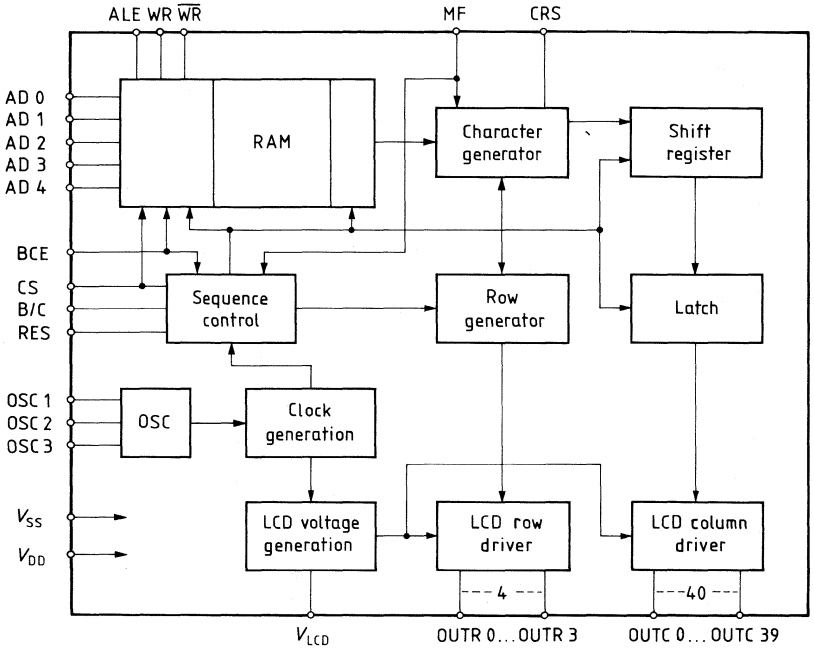
As the individual spools do not contain a constant number of components, smaller or larger quantities are possible as partial shipments of large quantities.

* For assembly instructions for MICROPACKs see page 11

Pin assignment

Pin No.	Designation	Pin No.	Designation
1	V_{DD}	33	OUT C26
2	V_{LCD}	34	OUT C27
3	OUT R0	35	OUT C28
4	OUT R1	36	OUT C29
5	OUT R2	37	OUT C30
6	OUT R3	38	OUT C31
7	OUT C0	39	OUT C32
8	OUT C1	40	OUT C33
9	OUT C2	41	OUT C34
10	OUT C3	42	OUT C35
11	OUT C4	43	OUT C36
12	OUT C5	44	OUT C37
13	OUT C6	45	OUT C38
14	OUT C7	46	OUT C39
15	OUT C8	47	CS
16	OUT C9	48	AD0
17	OUT C10	49	AD1
18	OUT C11	50	AD2
19	OUT C12	51	AD3
20	OUT C13	52	AD4
21	OUT C14	53	RES
22	OUT C15	54	WR
23	OUT C16	55	$\overline{WR}$
24	OUT C17	56	ALE
25	OUT C18	57	BCE
26	OUT C19	58	CRS
27	OUT C20	59	V_{SS}
28	OUT C21	60	MF
29	OUT C22	61	B/C
30	OUT C23	62	OSC 1
31	OUT C24	63	OSC 2
32	OUT C25	64	OSC 3

Figure 1
Block diagram



Functional description
(fig. 1 and pin designation)

The PSB 7510 controls LCDs in a quadruple mux mode.
The inputs AD0...AD4 accept the display address and display data in binary code. The display address is latched with ALE and used to address an internal RAM. The data is then stored in the internal RAM using $\overline{WR}$ control signal (**fig. 2**). The further translation of the display address and data in the RAM is asynchronous to the external control signals and is done internally using an on-chip oscillator.

In each mux step the character ROM translates the RAM contents and loads the result into a shift register. At the end of each mux phase the shift register is latched and used to control the bidirectional switches for the LCD drive signals. The LCD voltages are

generated from the input voltage V_{LCD} by an integrated resistor network. Polarity as well as magnitude of the actual LCD voltage for the output analog drivers is provided by a low-resistive switching network.

The IC additionally features underscoring of selected digits by blinking or cursor.

Input B/C selects blinking or cursor and is enabled with blink or cursor enable BCE.

Pin designation

Pin No.	Symbol	Description
1	V_{DD}	Positive supply voltage
2	V_{LCD}	LCD input voltage
3	OUT R0	Output row drivers
.	.	
.	.	
.	.	
6	OUT R3	
7	OUT C0	Output column drivers
.	.	
.	.	
.	.	
46	OUT C39	
47	CS	Chip select
48	AD0	Binary inputs for address and data
.	.	
.	.	
.	.	
52	AD4	
53	RES	Reset
54	WR	Write data latch enable (non-inverting)
55	$\overline{WR}$	Write data latch enable (inverting)
56	ALE	Address latch enable
57	BCE	Blink and cursor enable
58	CRS	Character ROM select
59	V_{SS}	Ground
60	MF	Selection of multiple flag
61	B/C	Blink or cursor function select
62	OSC1	Oscillator inputs
.	.	
.	.	
.	.	
64	OSC3	

Logic type

Positive logic is used
V_{DD} = "H" high level = logical 1 = positive voltage
V_{SS} = "L" low level = logical 0 = negative voltage

1. Chip select CS

The PSB 7510 responds to external signals only when CS is activated.

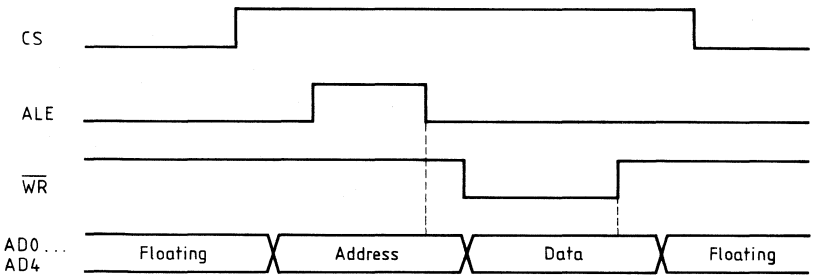
2. Reset RES

Reset clears the display and fills the internal RAM with blanks.

3. Address and data input AD0...AD4

The address pending AD0...AD4 is latched with the trailing edge of ALE. After this address assignment, the display data pending at AD0...AD4 is read into the RAM with the trailing edge of $\overline{WR}$ (**fig. 2**). The inputs use binary code.

Figure 2



4. Multiple flag MF (internal high-resitive connection with V_{DD})

When MF = 1, normal data input can be used to set one flag per digit at any desired position of the display. The character set automatically specified by MF = 1 (set I) comprises the characters 0...9, 3 bars and a blank. In this case, the character ROM select CRS input is "don't care".

The selected locations are specified by writing a "1" into the unused fifth data bit for this character set (set I).
When a character with a flag is changed, the flag must also be rewritten.

5. Select of character set CRS (internal high-resistive pullup resistor)

Input CRS is used to select the character set I or II, when MF = 0

Set I: CRS = 0
Set II: CRS = 1

6. Blink or cursor function select B/C (internal high-resistive pullup resistor) with V_{DD}.

The input selects whether a digit is to be highlighted in the display by blinking or by a cursor.

Blinking: B/C = 1
Cursor: B/C = 0

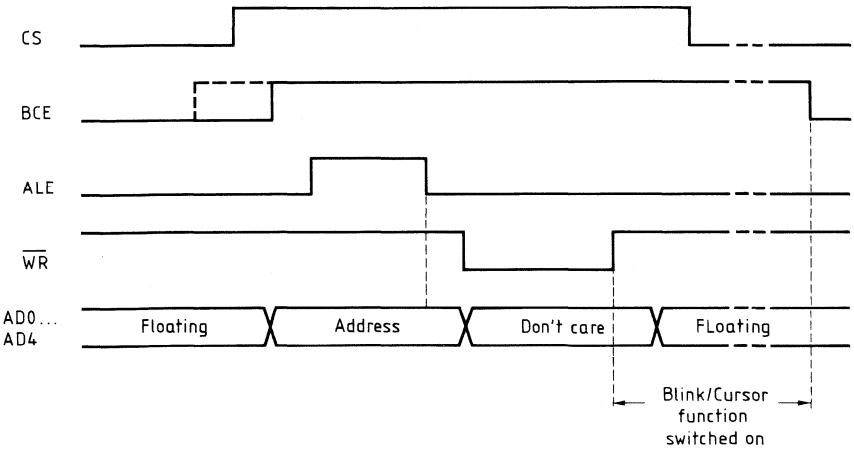
When using the blink option with characters with a flag, the flag blinks as well. The cursor option is not available for characters with a flag.

7. Blink or cursor function enable BCE

BCE = 1 enables the blinking or the cursor function (**fig. 3**). The address of the character in the display that is to be highlighted is latched with the falling edge of ALE.
ALE must be followed by a WR signal.
Following data information is "don't care".
This function can only be stopped with BCE = 0.
Reset RES has no effect.
Characters can only be changed when this function is disabled. After a character change, the blinking or cursor address must be given again. The blink or cursor function is available only for one digit at a time.

Figure 3

Blink/cursor functions switched on

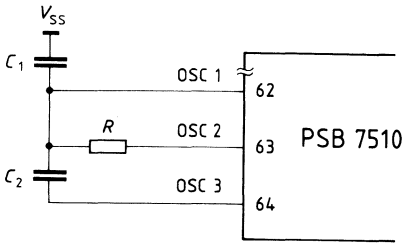


8. Oscillator inputs OSC 1, OSC 2 and OSC 3

The *RC* circuitry of these inputs determines the frequency of the oscillator. With an oscillator frequency of 25.6 kHz, the refresh rate is 40 Hz. (**refer** to **fig. 4**).

Figure 4

***RC* circuitry of oscillator inputs**



Suggested values: $R \approx 270\,k\Omega$
$C_1, C_2 \approx 47pF$

9. LCD voltage V_{LCD}

This voltage is applied board-externally and is divided by an integrated resistor network into the optimum interim values.

10. Output drivers

They provide the analog voltages for the LC-display

Maximum ratings

Input voltages	V_{max}	V_{DD} + 0.3	V
	V_{min}	−0.3	V

Operating range

Supply voltages	V_{DD}	2.5 to 6	V
	V_{SS}	0	V
LCD voltage		$V_{SS} \leq V_{LCD} \leq V_{DD}$	
Operating temperature	T_{amb}	0 to 70	°C

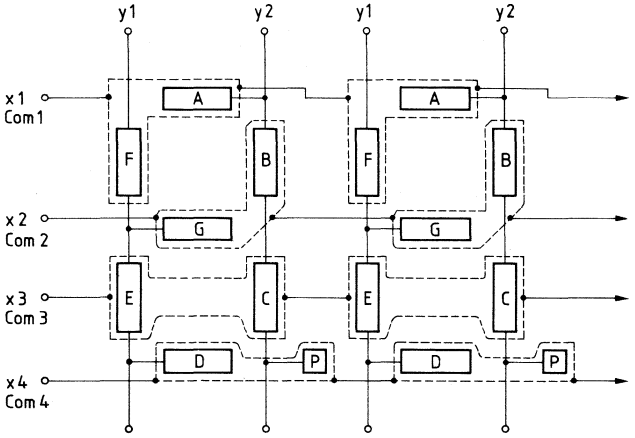
Display input data

Data	Display		Address	Address code
	Set I	Set II		
00000	0	0	0	00000
00001	1	1	1	00001
00010	2	2	2	00010
00011	3	3	3	00011
00100	4	4	4	00100
00101	5	5	5	00101
00110	6	6	6	00110
00111	7	7	7	00111
01000	8	8	8	01000
01001	9	9	9	01001
01010	bar above	bar above	10	01010
01011	bar center	bar center	11	01011
01100	bar below	A	12	01100
01101		B	13	01101
01110		C	14	01110
01111	blank	D	15	01111
10000		blank	16	10000
			17	10001
			18	10010
			19	10011

Input of an undefined data word causes a blank to be displayed at the respective display location.

Figures 5

Liquid crystal matrix organization



	y1	y2
x1	F	A
x2	G	B
x3	E	C
x4	D	P

Data Store
2048 Bit Static CMOS Memory (256x8)

SAB 81C50
(SM 852)

Preliminary data

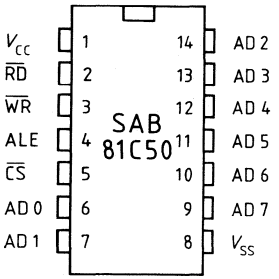
MOS circuit

Type	Ordering code	Package outline
SAB 81C50	Q 67100-Z 156	DIP 14

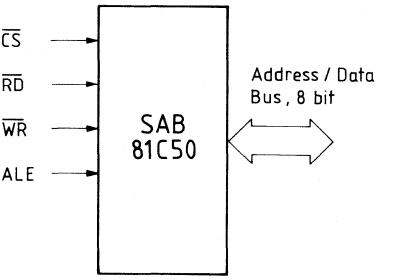
The SAB 81C50 is a 2048 bit static random access memory (RAM), organized as 256 words by 8 bits, manufactured using CMOS silicon gate technology. The multiplexed address and data bus allows to interface directly with the CMOS 8 bit organized processors and microcomputers, for example with SAB 8085, SAB 8086, SAB 8088, SAB 8048, SAB 80C48, SAB 8051 and SAB 80C482. Low standby power dissipation ($< 1\,\mu A$) minimizes system power requirements.

- 256×8 bit organization
- Low power dissipation
- Multiplexed address and data bus
- Single supply voltage 2.5 V to 6 V
- Tristate address/data lines
- On-chip address register
- Only 1 μA standby current

Pin configuration
top view



Logic symbol



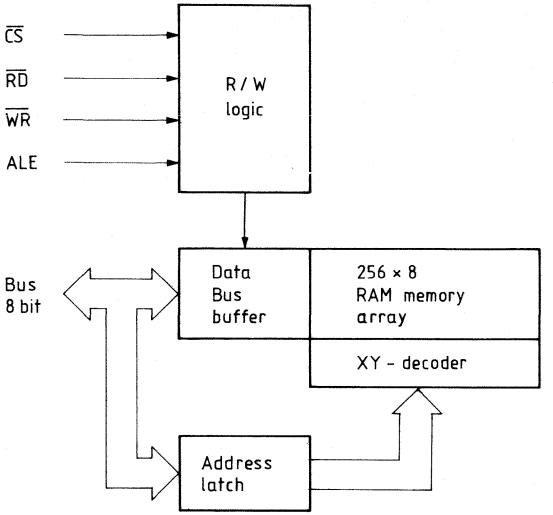
Pin designation

Pin No.	Symbol	Description
2	$\overline{RD}$	Read enable
3	$\overline{WR}$	Write enable
4	ALE	Address latch enable
5	$\overline{CS}$	Chip select (low = active, high = standby state)
6 ... 7 9 ... 14	AD0...AD7	Address/data lines
1	V_{CC}	Power supply (+5V)
8	V_{SS}	Circuit GND potential (0 V)

Truth table for control and data bus pin status

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	AD0...AD7 during data portion of cycle	Function
H	X	X	floating	no function
L	L	H	data from memory	read
L	H	L	data to memory	write
L	H	H	floating	no function

Block diagram



Maximum ratings

Ambient temperature under bias	T_{amb}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Voltage at any pin with respect to GND (V_{SS})	V	0 to 7	V
Total power dissipation	P_{tot}	250	mW

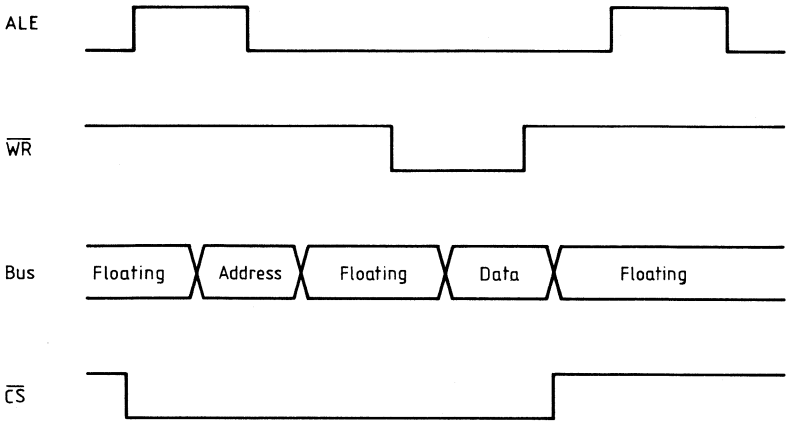
DC characteristics

T_{amb} = 25°C; V_{CC} = 2.5 V to 6 V; V_{SS} = 0 V

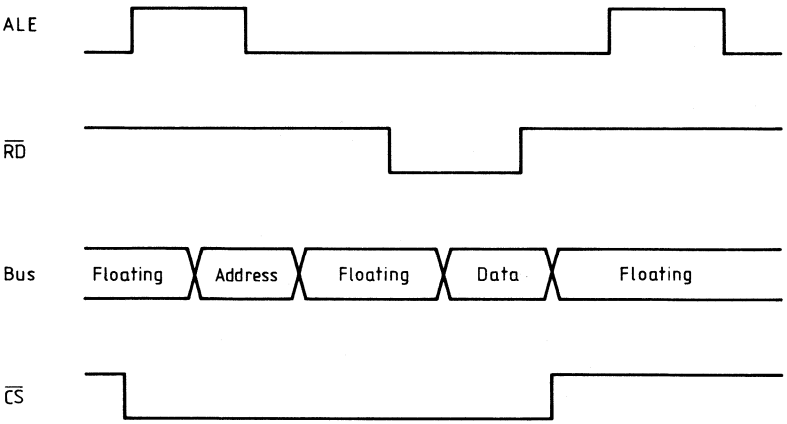
		Test conditions	Min.	Max.	Unit
Standby supply current	I_{CC}			1	µA
Operating supply current	I_{CC}	f = 1 MHZ		500	µA

Timing waveforms

Read



Write



Station Interface Digital (STID)

PSB 3530
(SM 339)

Preliminary data

MOS circuit

Type	Ordering code	Package outline
PSB 3530	Q 67100–Y646	DIC 28

Features

- Digital interface for time multiplexed 2-wire telephone sets
- Data rate 64 Kbit/s
- Outband signaling 8 Kbit/s
- Clock generation for STID, CODEC and μC
- Synchronization to PABX
- Interface between line (burst structure of data), CODEC (PCM), signaling (μC bus) and data terminal (serial I/O-port)
- Low radio frequency interference (RFI); fulfills N-12-specification

Application

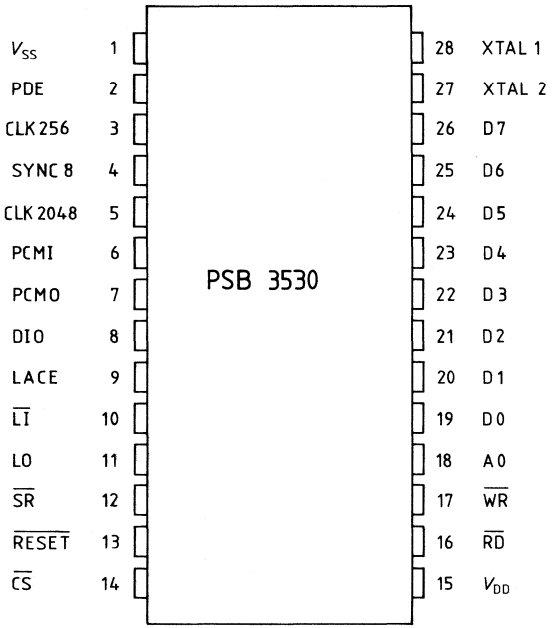
- Digital telephone sets
- Data terminals with digital links

General description

The Siemens station interface digital (STID) PSB 3530 is a monolithic NMOS circuit. It is the central interface device for the Digital Telephone Set. It connects the time multiplexed 2-wire line ("ping pong") to the subscriber apparatus.

A block diagram of a digital telephone system using the PSB 3530 is shown in **figure 1.**

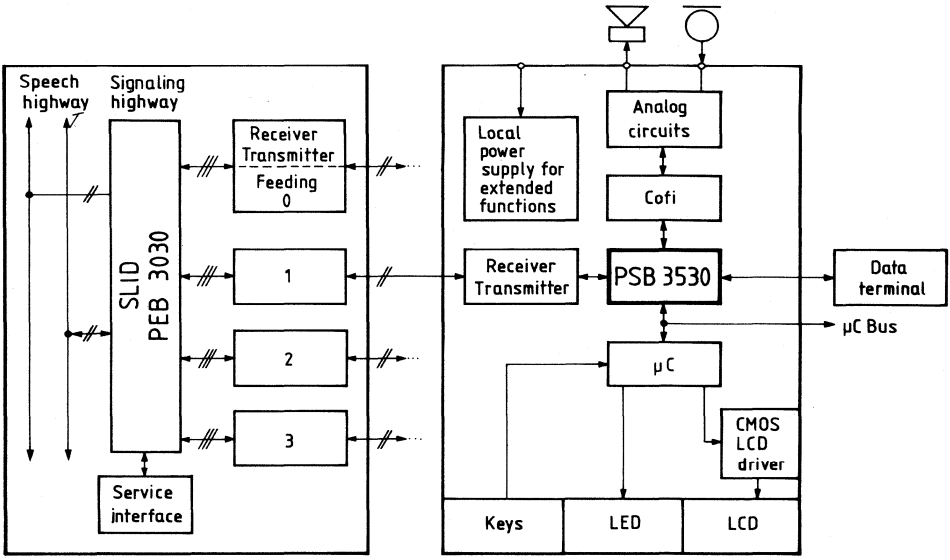
Pin configuration
top view



Pin designation

Pin No.	Symbol	Description
1	V_{SS}	GND
2	PDE	Power down enable
3	CLK 256	256 kHz clock output
4	SYNC 8	Sync. signal output, 8 kHz
5	CLK 2048	2.048 MHz clock output
6	PCMI	PCM input
7	PCMO	PCM output
8	DIO	Data serial input/output
9	LACE	AGC (automatic gain control) to receive/transmit-IC
10	$\overline{LI}$	Line input from receive/transmit-IC
11	LO	Line output to receive/transmit-IC
12	$\overline{SR}$	Signaling ready (interrupt for µC, 1 ms)
13	$\overline{RESET}$	Reset for µC
14	$\overline{CS}$	Chip select
15	V_{DD}	Supply voltage +5V
16	$\overline{RD}$	Read input
17	$\overline{WR}$	Write input
18	A0	Address input
19	D0	8 bit parallel data bus 3-state capability for signaling with µC
20	D1	
21	D2	
22	D3	
23	D4	
24	D5	
25	D6	
26	D7	
27	XTAL 2	XTAL terminals 8.192 MHz
28	XTAL 1	

Figure 1
Block diagram of a digital telephone system



Functional description

Figure 2 shows the block diagram of the internal circuits of the STID PSB 3530 with the four bidirectional data interfaces. The PBS 3530 has an on-chip XTAL-controlled oscillator of 8.192 MHz, from which all clocks for the connected equipment are derived. The PSB 3530 synchronizes with the PABX, stores the incoming burst every 250 µs (**fig. 3**). It also controls the sync-bit and separates the PCM data and the signaling information. It exchanges the PCM information with the CODEC every 125 µs and the signaling information via a µC bus every 1 ms in a parallel byte format.

At the serial interface DIO (**fig. 3**) every 125 µs one PCM word from the line and one from the CODEC are sent to the data terminal. Time interleaved, two words are taken from that interface for the line and the CODEC and are used in the data operation mode only (**fig. 4**). For the transmission to the PABX the STID compiles the 20 bit burst from PCM-, signaling- and synchronization information.

Figure 2
Block diagram

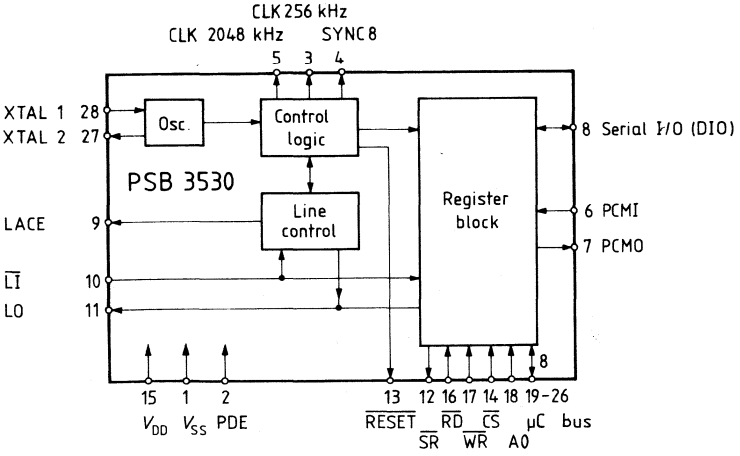


Figure 3
Data format and timing

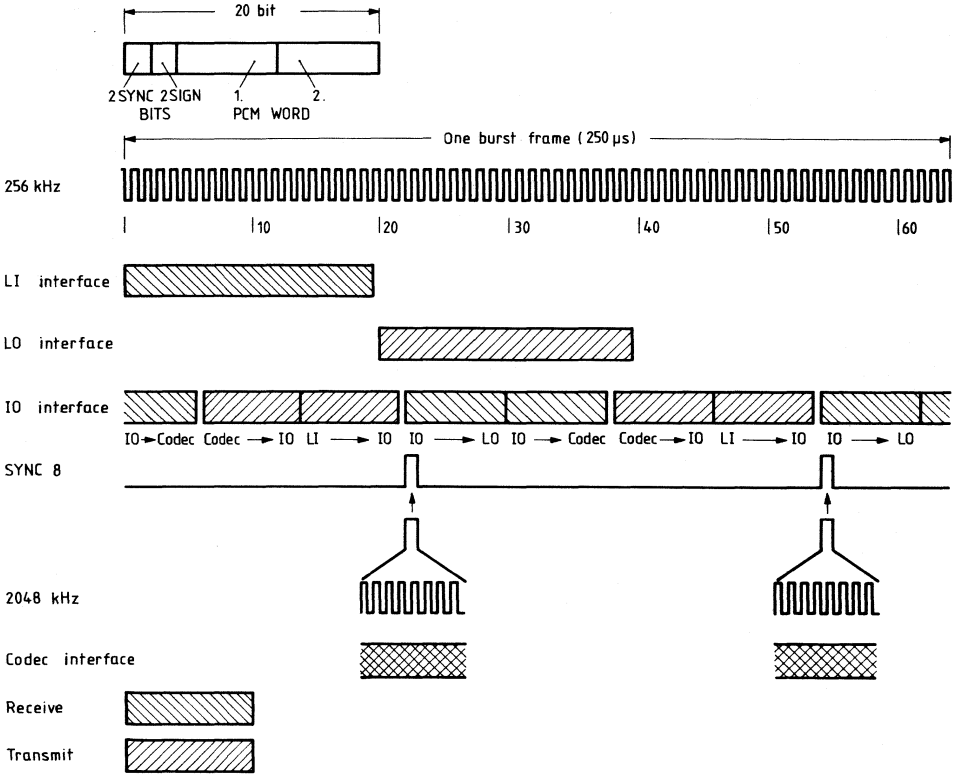
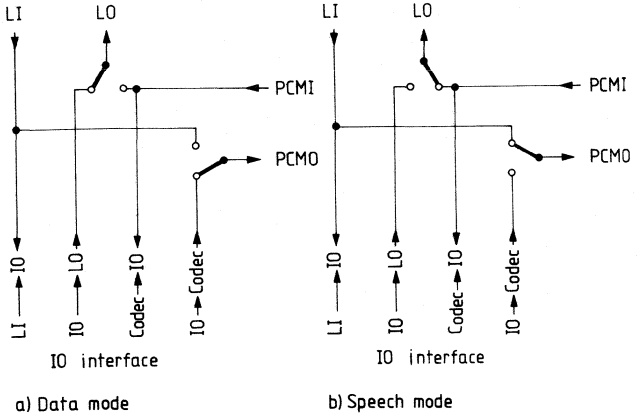


Figure 4
Operation in PCM and DATA mode



Maximum ratings

		Min.	Max.	Unit
Supply voltage	V_{DD}	−0.3	7	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	−55	125	°C
Total power consumption	P_{tot}		1	W
Input voltage	V_I	−0.3	7	V

Electrical characteristics

(T_{amb} = 0 to 70°C)

		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Supply current	I_{DD}	2	4	8	mA
Input current	I_I			10	µA
H input voltage	V_{IH}	2.4			V
L input voltage	V_{IL}			0.8	V
L output voltage	V_{OL}			0.4	V
H output voltage	V_{OH}	3.5			V

ICs for Telephone Exchanges

Preliminary data **MOS circuit**

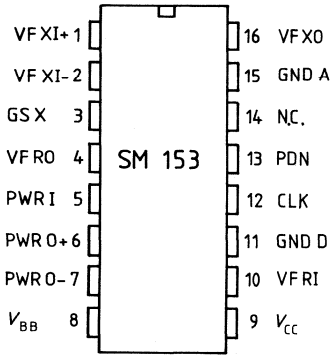
Type	Ordering code	Package outline
SM 153	Q 67100–Y 606	DIC 16

Features

- Monolithic device in NMOS, double-poly-Si-technology
- Transmit and receive filter in one 16 pin package
- Pin-compatible to Intel 2912, Mostek MK 5912, NS TP 3040 (at 2.048 MHz)
- No external filter adjustment required
- CCITT G 712 compatible
- $16^2/_3$ Hz, 50 Hz, 60 Hz attenuation in transmit filter
- Anti-aliasing filter in transmit section
- Gain adjustment in both directions by external resistors
- Power supplies +5V, −5V (±5%)
- Typ. power consumption
  130 mW without driver stage
  170 mW with driver stage
  50 mW in power down mode
- Clock- and control-input TTL-compatible
- Direct interfacing with transformer or electronic hybrids
- Clock 2.048 MHz
- Is designed to be used with the Siemens CODEC SM 61 C, Intel Codec 2910 A/2911 A, Mostek MK 5165, and others.

Pin configuration

top view

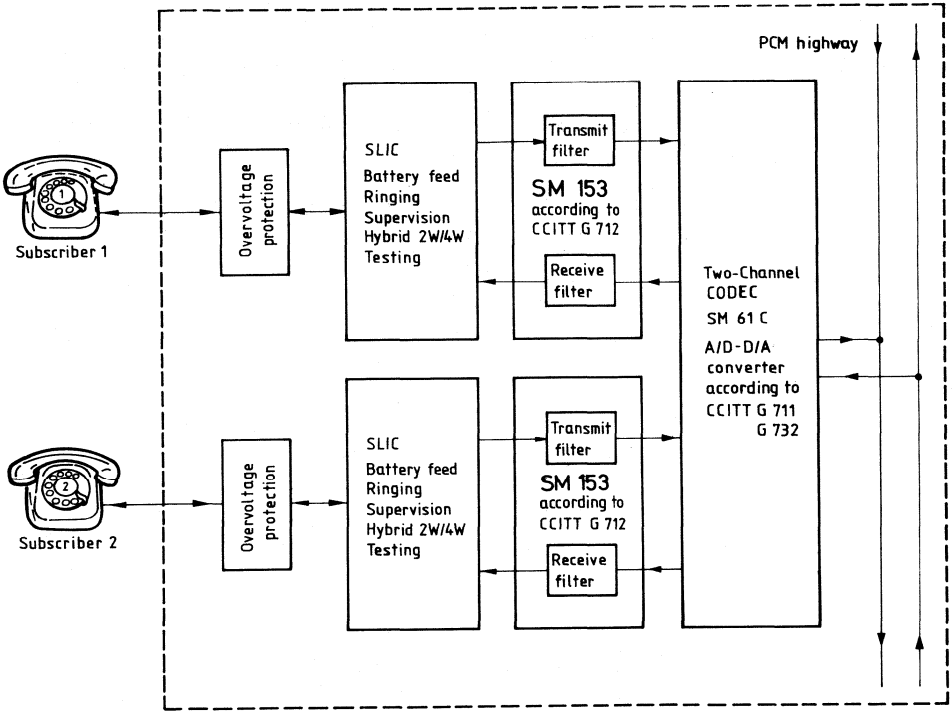


General description

The PCM filter SM 153 is a monolithic NMOS circuit containing the transmit and receive filter and the driver stage. The filter meets the CCITT G 712 recommendations. The device has a low power consumption and is a low-cost alternative to hybrid filters. The PCM filter is compatible with the filters Intel 2912, Mostek MK 5912, NS TP 3040 at 2.048 MHz.

Figure 1 shows a PCM system block diagram using the switched capacitor filter SM 153, a SLIC and the Two-Channel-CODEC SM 61 C.

Figure 1
PCM system block diagram



Functional description

Figure 2 shows the block diagram of the PCM filter and the external connections.

Transmit section

The input stage of the transmit filter consists of an operational amplifier with gain adjustment (gain = $1+R_2/R_1$). The input signal on pin VFXI + can be AC or DC coupled. The internal anti-aliasing filter is a second order low pass filter. A second order high pass filter, which operates in a switched capacitor technique, rejects low frequency noise. The fifth order low pass filter in switched capacitor technique operates with 256 kHz clocks. This filter is followed by a second order output smoothing filter. The transmit filter transfer characteristic in shown in **figure 3.**

The voltage range of transmit filter output signal is ±3.2V. The DC voltage offset is less than 250 mV. Therefore, it is recommended that the filter output signal is capacitively coupled to the PCM CODEC SM 61 C.

Receive section

The receive filter consists of a fifth order low pass switched capacitor and a sinx/x correction network. The receive filter transfer characteristic is shown in **figure 4.** The tolerances relate to a typical receive filter transfer characteristic, which is multiplied by the decoder attenuation/frequency distortion $\frac{\sin(\pi f/8000)}{\pi f/8000}$.

The receive filter output stage at VFRO provides a direct interface to high impedance circuits ($R_L > 10$ kΩ). The resistor voltage divider R_3 and R_4 is used for the filter gain adjustment in the receive direction. For a 10 kΩ load resistor connected between pin VFRO and ground the output voltage swing is ±3.2V.

Balanced driver stage

The receive filter output can be connected to the balanced driver amplifier stage to drive low impedance loads. A typical connection of the driver stage is shown in **figure 5.** With a load of 600 Ω connected between the signal outputs PWRO+ and PWRO− the voltage swing is ±5.0V. For reduced power dissipation the driver stage should be deactivated, when not utilized, by connecting the input PWRI to V_{BB}.

Power supply

A high level on the power down input (pin 13) sets the PCM filter in the power down mode.

Typical application

Figure 6 shows a typical application of the PCM filter SM 153 in connection with the PCM CODEC SM 61 C.

Figure 2
Block diagram

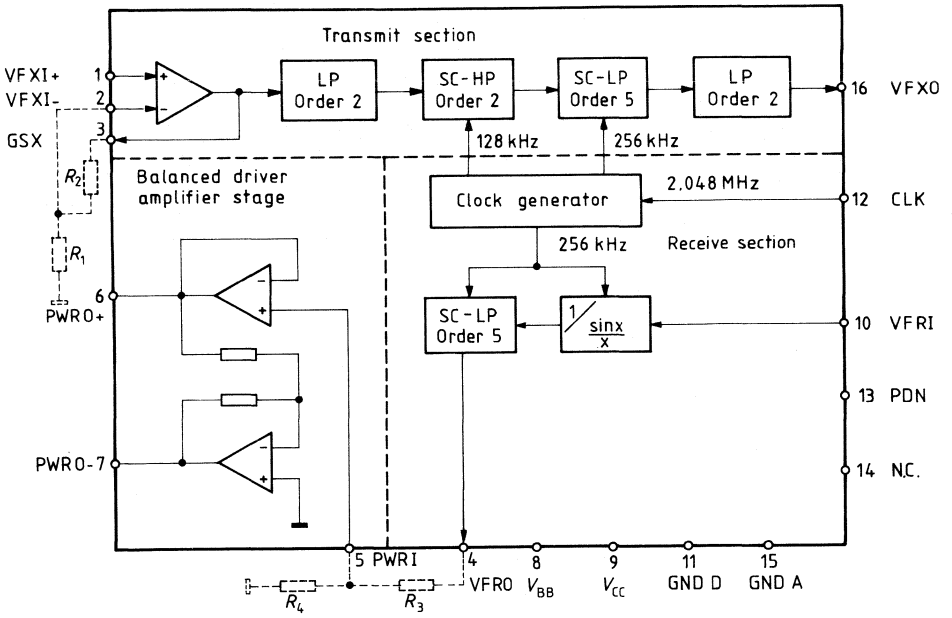


Figure 3

Transmit filter transfer characteristics

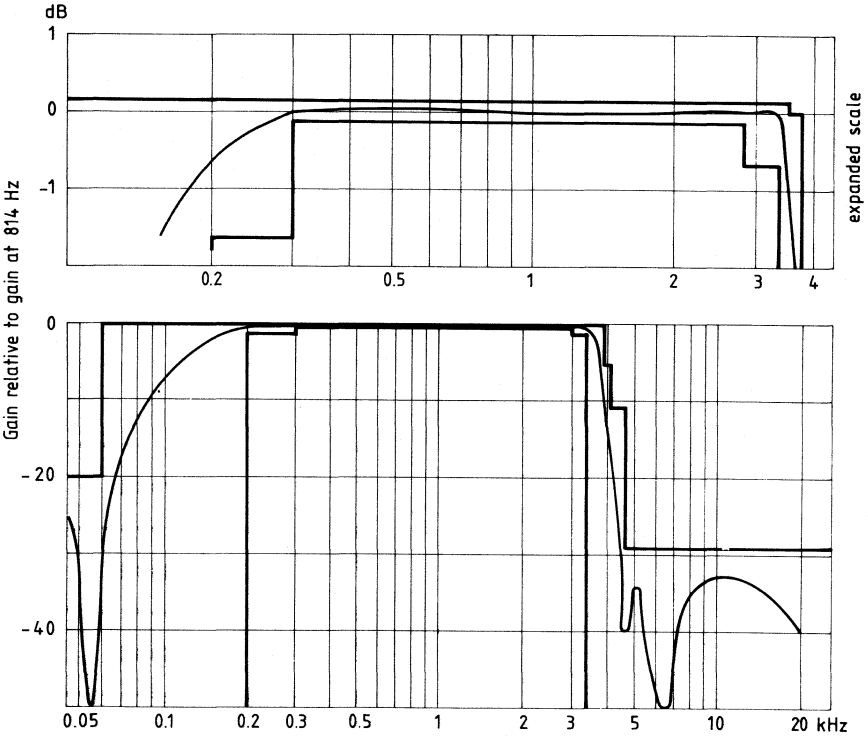


Figure 4

Receive filter transfer characteristics (when multiplied by sinx/x)

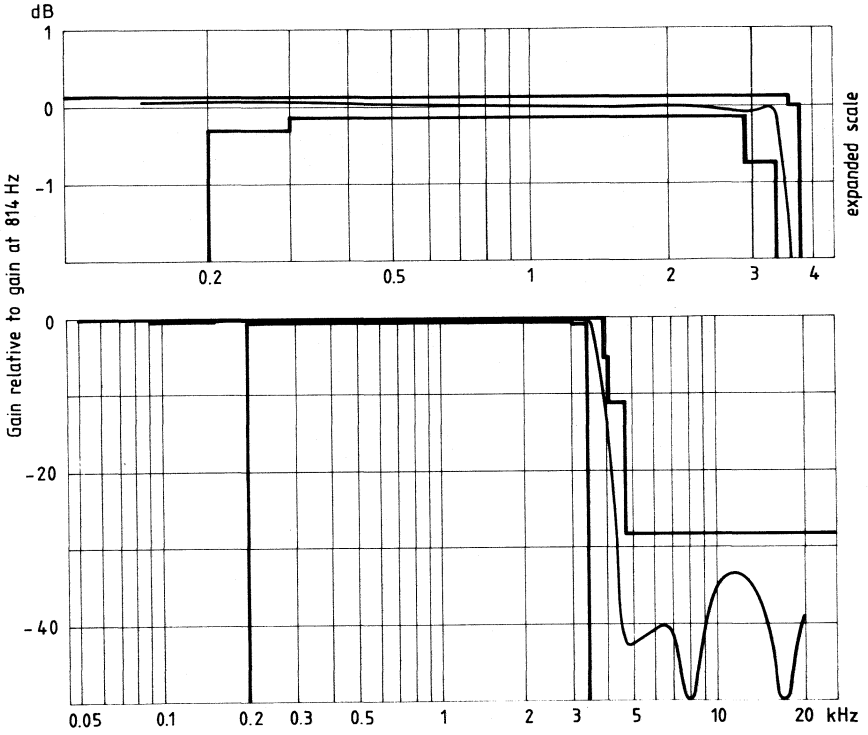


Figure 5
Typical connection of driver stage

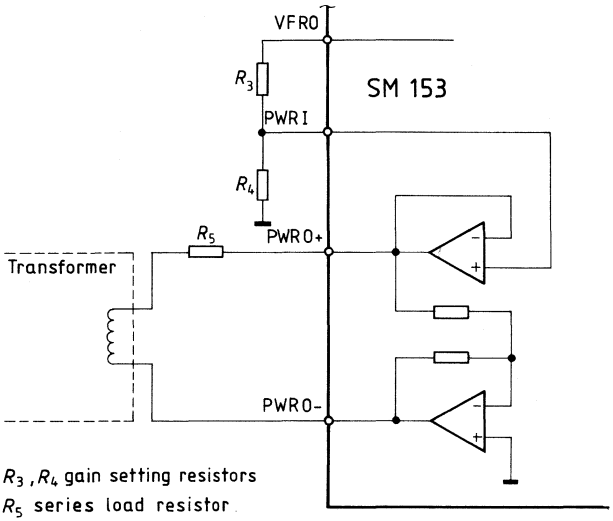


Figure 6

Typical application: Two PCM filters SM 153 and PCM CODEC SM 61 C

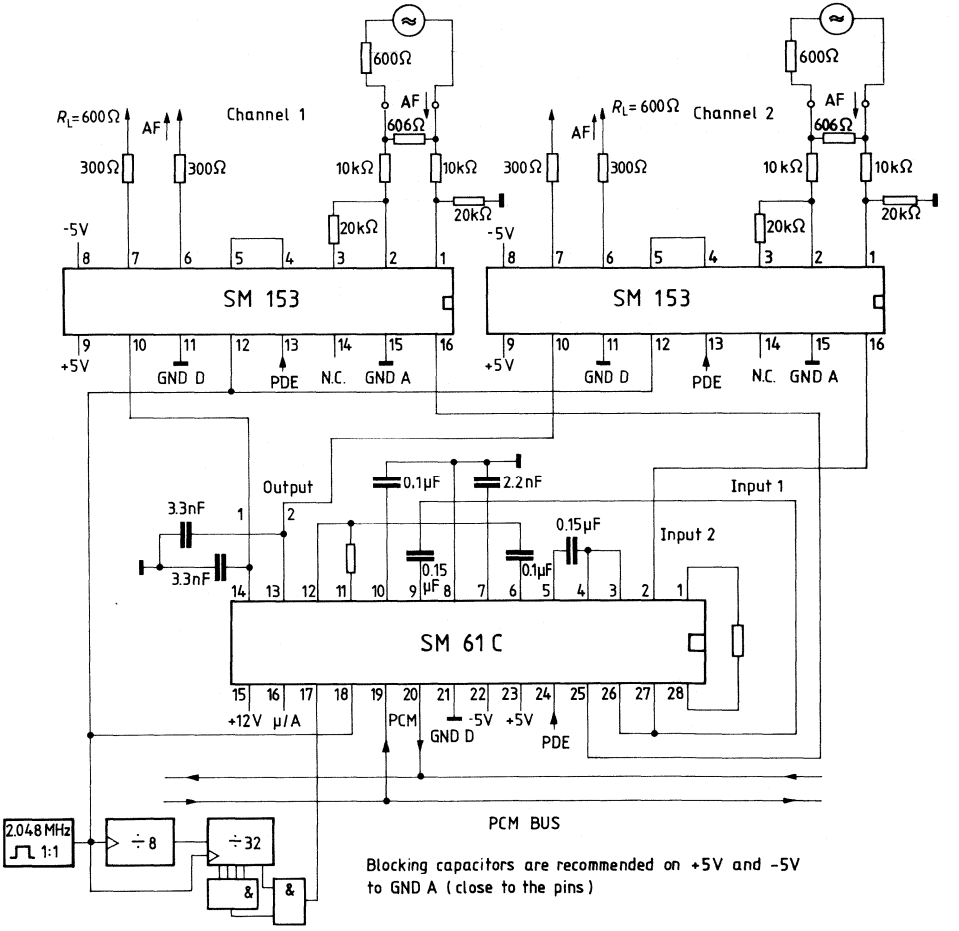
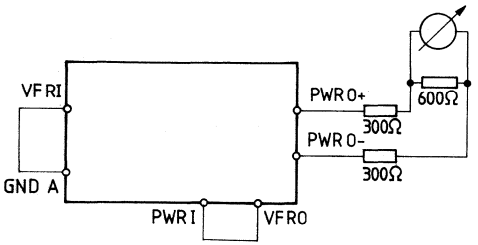


Figure 7

Test figure Receive filter idle noise measurement



Pin designation

Pin No.	Symbol	Description
1	VFXI+	Analog input of the transmit filter
2	VFXI−	Inverting input of the gain adjustment operational amplifier on the transmit filter
3	GSX	Output of the gain adjustment operational amplifier on the transmit filter
4	VFRO	Analog output of the receive filter
5	PWRI	Input to the power driver amplifiers for interfacing with hybrids
6	PWRO+	Non-inverting output of the power amplifiers
7	PWRO−	Inverting output of the power amplifiers
8	V_{BB}	−5 V ± 5% referenced to GND A
9	V_{CC}	+5 V ± 5% referenced to GND A
10	VFRI	Analog input of the receive filter
11	GND D	Digital ground
12	CLK	Clock input, TTL voltage level
13	PDN	Control input for the power down mode, TTL voltage levels
14	N.C.	Not connected
15	GND A	Analog ground
16	VFXO	Analog output of the transmit filter

Maximum ratings

		Min.	Max.	Unit
Supply voltage (relative to GND D)	V_{BB}	−10	0	V
	V_{CC}	−0.3	10	V
Output currents	I_O	−50	50	mA
Input and output voltages (relative to GND A)	V_I; V_O	−0.3	10	V
Operating temperature	T_{amb}	−25	75	°C
Storage temperature	T_{stg}	−55	125	°C
Total power dissipation	P_{tot}		600	mW

All inputs and outputs are protected against static discharges.

DC and operating characteristics

(V_{BB} = −5 V ± 5%, V_{CC} = +5 V ± 5%, f_{CL} = 2.048 MHz, T_{amb} = 0°C to 70°C)

Power interface		Test conditions	Min.	Typ.	Max.	Unit
Standby current	$I_{BB\,C}$	PDN = $V_{IH\,min}$			9	mA
Standby current	$I_{CC\,C}$				9	mA
Operating current power amplifier inactive	$I_{BB\,1}$	PWRI = V_{BB}			21	mA
Operating current power amplifier inactive	$I_{CC\,1}$	PWRI = V_{BB}			21	mA
Operating current	$I_{BB\,2}$				30	mA
Operating current	$I_{CC\,2}$				30	mA
Digital interface						
L input voltage	V_{IL}				0.8	V
H input voltage	V_{IH}		2.0			V
Input load current, CLK	I_{ILO}	V_{IN} = $V_{IL\,min}$ to $V_{IH\,max}$			10	µA
Input load capacitance, CLK	C_{ILO}			5	20	pF
Input load current, PDN	I_{ILO}	V_{IN} = $V_{IL\,min}$ to $V_{IH\,max}$			100	µA
Analog interface, transmit filter gain setting stage						
Input leakage current, VFXI+, VFXI−	I_{BXI}	−2.2 V < V_{IN} < 2.2 V			100	nA
Input resistance, VFXI+, VFXI−	R_{IXL}		10			MΩ
Input offset voltage, VFXI+, VFXI−	$V_{IO\,XI}$	−2.2 V < V_{IN} < 2.2 V			25	mV
Common mode rejection, GSX VFXI+, VFXI−	CMR	−2.2 V < V_{IN} < 2.2 V	45			dB
Power supply rejection, V_{CC}	$PSRR_1$	1 kHz	45			dB
Power supply rejection, V_{BB}	$PSRR_2$	1 kHz	45			dB
DC open loop gain, GSX	G_{VO}		66			dB
Open loop unity gain bandwidth GSX	f_{OL}			2		MHz
Output voltage swing, GSX	V_{OXI}	$R_L \geqq$ 10 kΩ	±2.5			V
Load capacitance, GSX	C_{LXI}				20	pF
Minimum load resistance, GSX	R_{LXI}		10			kΩ

DC and operating characteristics

(V_{BB} = −5 V ± 5%, V_{CC} = +5 V ± 5%, f_{CL} = 2.048 MHz, T_{amb} = 0°C to 70°C)

Analog interface,transmit filter		Test conditions	Min.	Typ.	Max.	Unit
Output resistance, VFXO	R_{OX}	Input op amp at unity gain			400	Ω
Output DC offset, VFXO	$V_{O\,OX}$	VFXI+ = GND A			250	mV
Load capacitance, VFXO	C_{LX}				20	pF
Minimum load resistance, VFXO	R_{LX}		10			kΩ
Output voltage swing, VFXO	V_{OX}	$R_L \geqq 10$ kΩ	±3.2			V
Power supply rejection, V_{CC}	$PSRR_3$	1 kHz	25			dB
Power supply rejection, V_{BB}	$PSRR_4$	1 kHz	25			dB
Analog interface, receive filter						
Input leakage current, VFRI	I_{BR}	$-3.2\ V \leqq V_{IN} \leqq 3.2\ V$			3	μA
Input resistance	R_{IR}		1			MΩ
Output resistance	R_{OR}				100	Ω
Output DC offset	$V_{O\,OR}$	VFRI = GND A			200	mV
Load capacitance	C_{LR}				20	pF
Minimum load resistance	R_{LR}		10			kΩ
Output voltage swing	V_{OR}	$R_L \geqq 10$ kΩ	±3.2			V
Power supply rejection, V_{CC}	$PSRR_5$	1 kHz	25			dB
Power supply rejection, V_{BB}	$PSRR_6$	1 kHz	22			dB
Analog interface, receive filter power amplifier stage						
Input leakage current	I_{BRA}	$-3.2\ V \leqq V_{IN} \leqq 3.2\ V$			3	μA
Input resistance	R_{IRA}		10			MΩ
Output resistance	R_{ORA}			1		Ω
Output DC offset	$V_{O\,ORA}$	PWRI = GND A			75	mV
Load capacitance	C_{LRA}				100	pF
Output voltage swing across R_L PWRO+, PWRO− single ended connection	$V_{ORA\,1}$	$R_L \geqq 10$ kΩ	±3.2			V
		$R_L \geqq 600$ Ω	±2.9			V
		$R_L \geqq 300$ Ω	±2.5			V
Output voltage swing across R_L R_L connected between PWRO+ and PWRO− Balance output connection	$V_{ORA\,2}$	$R_L \geqq 600$ Ω	±5			V

AC characteristics

(V_{BB} = −5 V ± 5%, V_{CC} = +5 V ± 5%, f_{CL} = 2.048 MHz, T_{amb} = 0°C to 70°C)

Transmit filter		Test conditions	Min.	Typ.	Max.	Unit
Absolute passband gain at 814 Hz	G_{AX}	Gain setting op amp at unity gain, $R_L = \infty$	2.9	3.0	3.1	dB
Attenuation relative to 814 Hz						
16⅔ Hz	α_{RX}	0 dBm0		15		dB
50 Hz to 60 Hz		output signal =	20			dB
200 Hz		1.55 V_{rms} at VFXO	−0.2		+1.8	dB
300 to 2900 Hz			−0.2		+0.2	dB
3000 Hz to < 3400 Hz			−0.2		+0.75	dB
3600 Hz			0			dB
3800 Hz			6.25			dB
4000 Hz			12.5			dB
≧ 4600 Hz			28			dB
Idle noise, VFXO	N_{OX}	relative to 1.55 V_{rms} gain setting op amp at unity gain, VFXI+, = GND A			−79	dBm0p
Phase characteristic		(GSX to VFXO): non inverting				

Receive filter						
Absolute passband gain at 814 Hz	G_{AR}	$R_L = \infty$	−0.1	0	+0.1	dB
Attenuation relative to 814 Hz with sinx/x correction	α_{RR}					
200 Hz		0 dBm0	−0.2		+0.5	dB
300 to 2900 Hz		output signal =	−0.2		+0.2	dB
3000 to < 3400 Hz		1.55 V_{rms} at VFRO	−0.2		+0.75	dB
3600 Hz			0			dB
3800 Hz			6.25			dB
4000 Hz			12.5			dB
≧ 4600 Hz			28			dB
Idle noise	N_{OR}	relative to 1.55 V_{rms} see fig. 7			−79	dBm0p
Phase characteristic		(VFRI to VFRO):		inverting		

PCM Filter

PEB 2912 (SM 153 B)

Preliminary data

MOS circuit

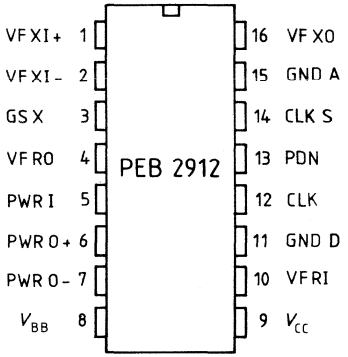
Type	Ordering code	Package outline
PEB 2912	Q67100-Z158	DIC 16

Features

- Monolithic device in NMOS, double-poly-Si-technology
- Transmit and receive filter in one 16 pin package
- Pin-compatible to Intel 2912, Mostek MK 5912, NS TP 3040
- No external filter adjustment required
- CCITT G 712 and AT & T D3/D4 compatible including the recommendations of the 4 wire - set - TMA
- $16^2/_3$ Hz, 50 Hz, 60 Hz attenuation in transmit filter
- Anti-aliasing filter in transmit and receive section
- Gain adjustment in both directions by external resistors
- Power supplies +5 V, −5 V (±5%)
- Low power consumption
  40 mW without driver stage
  55 mW with driver stage (level: 0 dBm, load : 600 Ω)
  <1 mW in power-down mode
- Clock- and control-input TTL-compatible
- Direct interfacing with transformer or electronic hybrids
- 1.536 MHz; 1.544 MHz; 2.048 MHz; 2.560 MHz clock
- Is designed to be used with the SIEMENS CODEC SM 61 C, Intel Codec 2910 A/2911 A Mosteck MK 5156, NS TP 3020

Pin configuration

top view

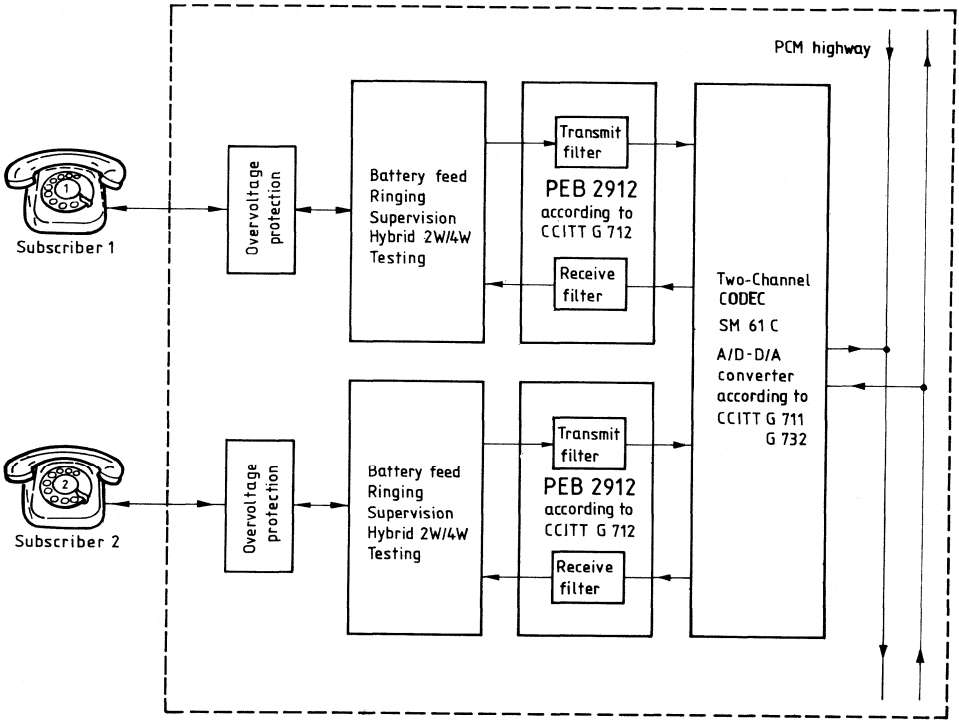


General description

The PCM filter PEB 2912 is a monolithic NMOS circuit containing the transmit and receive filters and the driver stage. The filter meets the CCITT G 712 and the AT & T D3/D4 recommendations. The device has a low power consumption and is a low cost alternative to hybrid filters. The PCM filter is compatible with the Intel filter 2912, Mostek MK 5912, NS TP 3040.

Figure 1 shows a PCM system block diagram using the switched capacitor filter PEB 2912, a SLIC and the Two-Channel CODEC SM 61 C.

Figure 1
PCM system block diagram



Functional description

Figure 2 shows the block diagram of the PCM filter and the external connections.

Transmit section

The input stage of the transmit filter consists of an operational amplifier with gain adjustment (gain = 1 + R_2/R_1). The input signal on pin VFXI+ can be AC-or DC-coupled. The internal anti-aliasing filter is a second order low pass filter. A third order high pass filter, which operates in a switched capacitor technique, rejects low frequency noise. The fifth order low pass filter in switched capacitor technique operates with 256 kHz clocks. This filter is followed by a second order output smoothing filter. The transmit filter transfer characteristics are shown in **figure 3.**

The voltage range of the transmit filter output signal is ±3.2 V. The DC voltage offset is less than 200 mV. Therefore, it is recommended that the filter output signal is capacitively coupled to the PCM CODEC SM 61 C.

Receive section

The receive filter consists of a fifth order low pass switched capacitor filter, a sinx/x correction network and a second order anti-aliasing filter. The receive filter transfer characteristics are shown in **figure 4.** The tolerances relate to a typical receive filter transfer characteristic, which is multiplied by the

decoder attenuation/frequeny distortion $\frac{\sin \pi\ (f/8000)}{\pi\ (f/8000)}$.

The receive filter output stage at VFRO, provides a direct interface to high impedance circuits (R_L > 10 kΩ). The resistor voltage divider R_3 and R_4 is used for the filter gain adjustment in the receive direction. For a 10 kΩ load resistor connected between pin VFRO and ground the output voltage swing is ±3.2 V.

Balanced driver stage

The receive filter output can be connected to the balanced driver amplifier stage to drive low impedance loads. A typical connection of the driver stage is shown in **figure 5.** With a load of 600 Ω connected between the signal outputs PWRO+ and PWRO− the voltage swing is ±5.0 V. For reduced power dissipation the driver stage should be reactivated, when not utilized, by connecting the input PWRI to V_{BB}.

Clock interface

An external clock is required which supplies the internal clock of 256 kHz.

CLK (Pin 12)	Bits/Frame	CLK S (Pin 14)
1.536 MHz	192	V_{BB}, −5 V
1.544 MHz	193	GND D
2.048 MHz	256	V_{CC}, +5 V
2.560 MHz	320	open circuit

Power supply

To improve the power supply rejection ratio (*PSRR*) an internal noise suppression circuit is provided to reject inband and outband noise on V_{CC} and V_{BB}.
A high level on the power down (pin 13) sets the PCM filter in the power down mode.

Typical application

Figure 6 shows a typical application of the PCM filter SM 153 B in connection with the PCM CODEC SM 61 C.

Figure 2
Block diagram

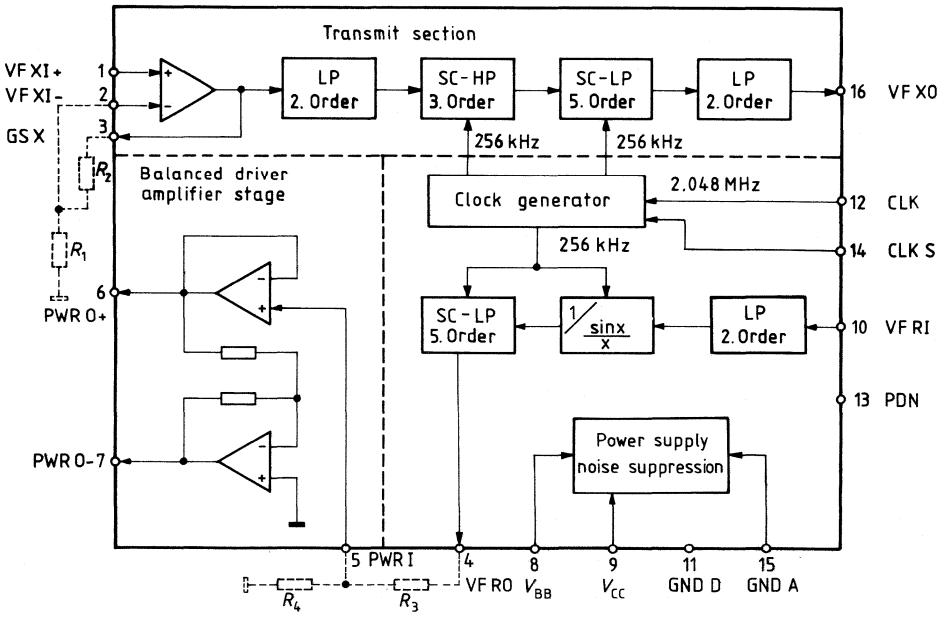


Figure 3

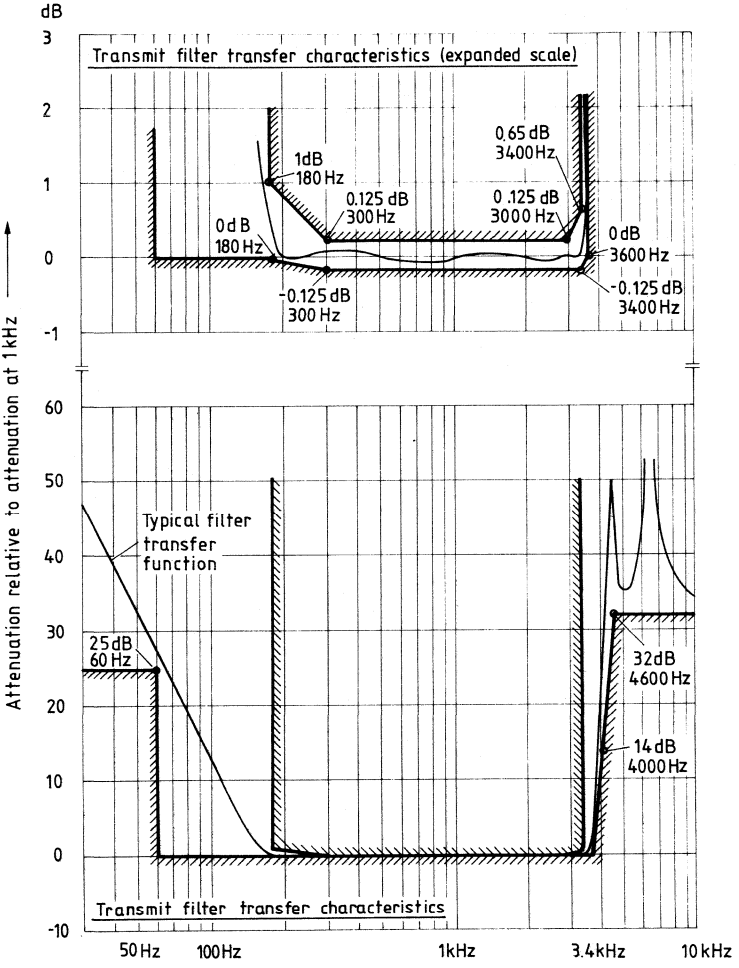

dB
3
2
1
0
-1
Transmit filter transfer characteristics (expanded scale)
1dB
180 Hz
0.125 dB
300 Hz
0.65 dB
3400 Hz
0.125 dB
3000 Hz
0dB
180 Hz
0dB
3600 Hz
-0.125 dB
300 Hz
-0.125 dB
3400 Hz
Attenuation relative to attenuation at 1 kHz
60
50
40
30
20
10
0
-10
Typical filter
transfer
function
25dB
60 Hz
32dB
4600 Hz
14dB
4000 Hz
Transmit filter transfer characteristics
50 Hz
100 Hz
1kHz
3.4kHz
10 kHz

Figure 4

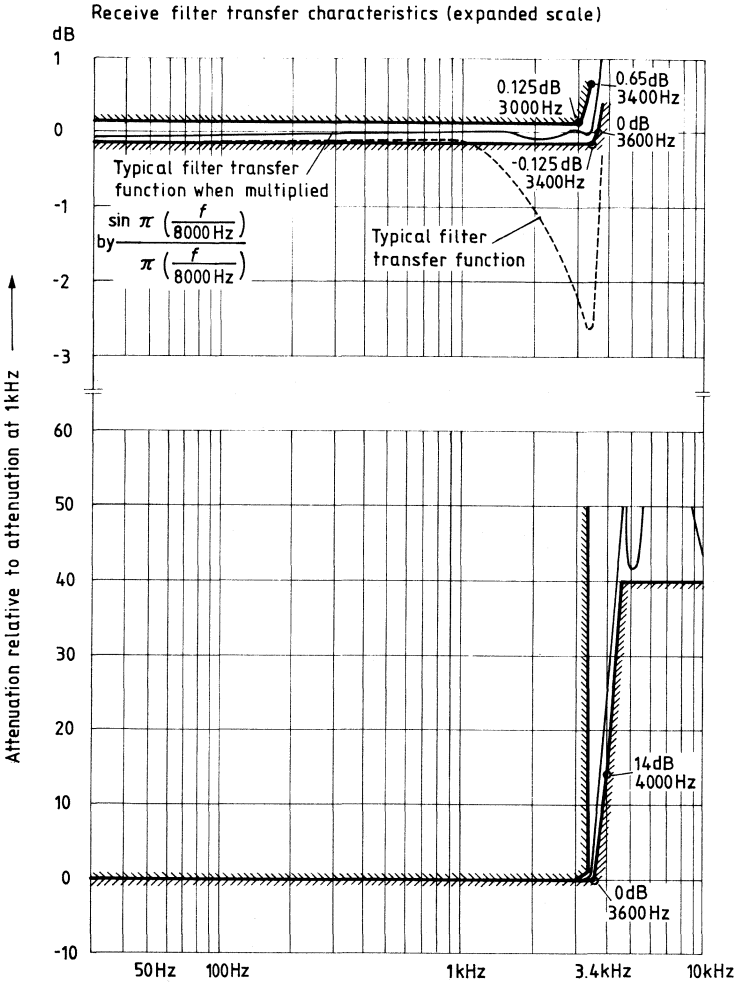

Receive filter transfer characteristics (expanded scale)
dB
1
0
-1
-2
-3
60
50
40
30
20
10
0
-10
0.125dB
3000Hz
0.65dB
3400Hz
0dB
3600Hz
-0.125dB
3400Hz
Typical filter transfer function when multiplied by
sin π (f/8000Hz) / π (f/8000Hz)
Typical filter transfer function
14dB
4000Hz
0dB
3600Hz
50Hz
100Hz
1kHz
3.4kHz
10kHz
Attenuation relative to attenuation at 1kHz
Receive filter transfer characteristics

Figure 5
Typical connection of driver stage

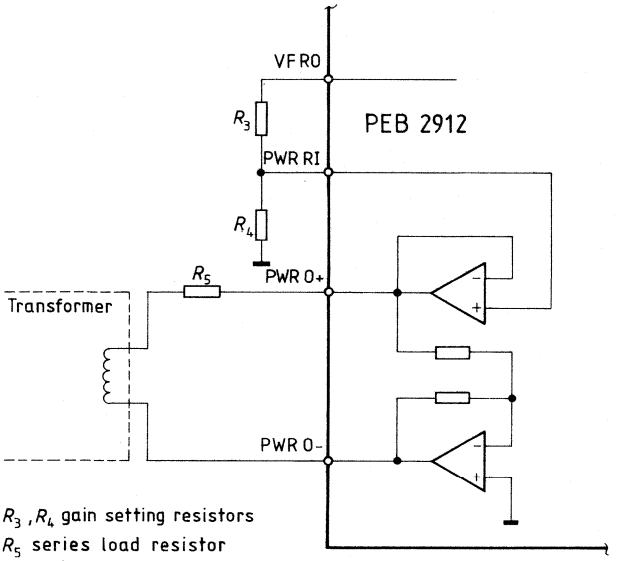
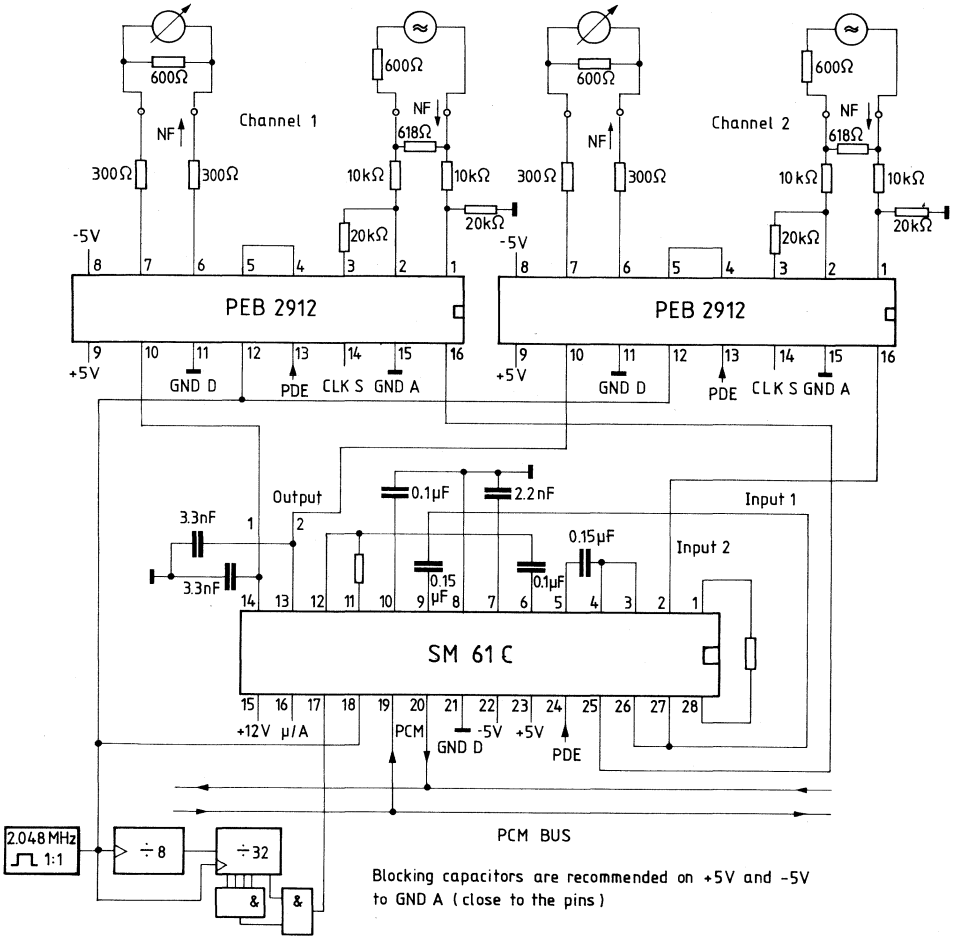


Figure 6

Typical application: Two PCM filters PEB 2912 and PCM CODEC SM 61 C



Pin designation

Pin No.	Symbol	Description
1	VFXI+	Analog input of the transmit filter
2	VFXI−	Inverting input of the gain adjustment operational amplifier on the transmit filter
3	GSX	Output of the gain adjustment operational amplifier on the transmit filter
4	VFRO	Analog output of the receive filter
5	PWRI	Input to the power driver amplifiers for interfacing with hybrids
6	PWRO+	Non-inverting output of the power amplifiers
7	PWRO−	Inverting output of the power amplifiers
8	V_{BB}	−5 V ±5% referenced to GND A
9	V_{CC}	+5 V ± 5% referenced to GND A
10	VFRI	Analog input of the receive filter
11	GND D	Digital ground
12	CLK	Clock input, TTL voltage levels
13	PND	Control input for the power-down mode, TTL voltage levels
14	CLK S	Clock select input
15	GND A	Analog ground
16	VFXO	Analog output of the transmit filter

Maximum ratings

		Min.	Max.	Unit
Supply voltage	V_{BB}	−10	0	V
(relative to GND D)	V_{CC}	−0.3	10	V
Output current	I_O	−50	50	mA
Input and output voltages (relative to GND A)	V_I, V_O	−0.3	10	V
Operating temperature	T_{amb}	−25	75	°C
Storage temperature	T_{stg}	−55	125	°C
Total power dissipation	P_{tot}		600	mW

All inputs and outputs are protected against static discharges.

DC and operating characteristics

($V_{BB} = -5V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $\left|\frac{\Delta f_{CL}}{f_{CL}}\right| \leq 3 \cdot 10^{-4}$, $T_{amb} = 0°C$ to $70°C$

		Test conditions	Min.	Typ.	Max.	Unit
Power interface						
Standby current	I_{BBC}	PDN = $V_{IH\,min}$			100	µA
Standby current	I_{CCC}				100	µA
Operating current, power amplifier inactive	I_{BB1}	PWRI = V_{BB}		4		mA
Operating current, power amplifier inactive	I_{CC1}	PWRI = V_{BB}		4		mA
Operating current	I_{BB2} *)			5.5		mA
Operating current	I_{CC2} *)			5.5		mA
Power supply rejection of V_{BB}	$PSRR_1$	at 1 kHz		40		dB
Power supply rejection of V_{CC}	$PSRR_2$	at 1 kHz		40		dB
Power supply rejection of V_{BB}	$PSRR_3$	0 to 160 kHz				dB
Power supply rejection of V_{CC}	$PSRR_4$	0 to 160 kHz				dB
Digital interface						
L input voltage (exept CLK S)	V_{IL}				0.8	V
H input voltage (exept CLK S)	V_{IH}		2.0			V
Input load current	I_{ILO}	$V_{IN} = V_{IL\,min}$ to $V_{IH\,max}$			10	µA
L input voltage, CLK S	$V_{IL\,S}$		V_{BB}		$V_{BB}+0.5$	V
Input intermediate voltage, CLK S	$V_{II\,S}$		GND D −0.5		0.2	V
H input voltage, CLK S	$V_{IH\,S}$		$V_{CC}-0.5$		V_{CC}	V
Input load capacitance, CLK				5		pF
Analog interface, transmit filter gain setting stage						
Input leakage current, VFXI+, VFXI−	I_{BXI}	$-2.2\,V < V_{IN} < 2.2\,V$			100	nA
Input resistance, VFXI+, VFXI−	R_{IXL}		10			MΩ
Input offset voltage, VFXI+, VFXI−	V_{IOXI}	$-2.2\,V < V_{IN} < 2.2\,V$			25	mV
Common mode rejection VFXI+, VFXI−	CMR	$-2.2\,V < V_{IN} < 2.2\,V$	60			dB
Power supply rejection, GSX	$PSRR_5$	at 1 kHz	60			dB
DC open loop gain, GSX	G_{VO}		66			dB
Open loop unity gain bandwidth, GSX	f_{OL}			2		MHz
Output voltage swing, GSX	V_{OXI}	$R_L \geqq 10$ kΩ			±2.5	V
Load capacitance, GSX	C_{LXI}				20	pF
Minimum load restistance, GSX	R_{LXI}		10			kΩ

*) 0dBm is delivered to 600Ω connected from PWRO+ to PWRO−

DC and operating characteristics

($V_{BB} = -5\ V \pm 5\%$, $V_{CC} = +5\ V \pm 5\%$, $\left|\frac{\Delta f_{CL}}{f_{CL}}\right| \leqq 3 \cdot 10^{-4}$, $T_{amb} = 0°C$ to $70\ °C$)

Analog interface, transmit filter

		Test conditions	Min.	Typ.	Max.	Unit
Output resistance	R_{OX}	Input op amp at unity gain			100	Ω
Output DC offset	V_{OOX}	VFXI+ = GND A			250	mV
Load capacitance	C_{LX}				20	pF
Minimum load resistance	R_{LX}		10			kΩ
Output voltage swing	V_{OX}	$R_L \geqq 10\ k\Omega$			±3.2	V

Analog interface, receive filter

Input leakage current	I_{BR}	$-3.2\ V < V_{IN} < 3.2\ V$			1	µA
Input resistance	R_{IR}		10			MΩ
Output resistance	R_{OR}				100	Ω
Output DC offset	V_{OOR}	VFRI = GND A			200	mV
Load capacitance	C_{LR}				20	pF
Minimum load resistance	R_{LR}		10			kΩ
Output voltage swing	V_{OR}	$R_L \geqq 10\ k\Omega$			±3.2	V

Analog interface, receive filter power amplifier stage

Input leakage current	I_{BRA}	$-3.2\ V < V_{IN} < 3.2\ V$			3	µA
Input resistance	R_{IRA}		10			MΩ
Output resistance	R_{ORA}			1		Ω
Output DC offset	V_{OORA}	PWRI = GND A			50	mV
Load capacitance	C_{LRA}				100	pF
Output voltage swing across R_L PWRO+, PWRO− single-ended connection	$V_{ORA\,1}$	$R_L \geqq 300\ \Omega$			±3.2	V
Output voltage swing across R_L R_L connected between PWRO+ and PWRO− Balanced output connection	$V_{ORA\,2}$	$R_L \geqq 600\ \Omega$			±6.4	V

AC characteristics

($V_{BB} = -5\,V \pm 5\%$, $V_{CC} = +5\,V \pm 5\%$, $\left|\frac{\Delta f_{CL}}{f_{CL}}\right| \leq 3 \cdot 10^{-4}$, $T_{amb} = 0\,°C$ to $70°C$, $R_L \geq 50\,k\Omega$)

Transmit filter		Test conditions	Min.	Typ.	Max.	Unit
Absolute passband gain at 1 kHz	G_{AX}	Gain setting op amp at unity gain	2.9	3.0	3.1	dB
Attenuation relative to 1 kHz						
0 to 60 Hz	α_{RX}	0 dBm0	+25	+30		dB
180 Hz		output signal =	0		+1	dB
300 to 3000 Hz		1.55 V_{rms} at VFXO	−0.125		+0.125	dB
3400 Hz			−0.125	+0.1	+0.65	dB
3600 Hz			0			dB
4000 Hz			+14			dB
≧ 4600 Hz			+32			dB
Cross talk, attenuation receive to transmit at 1kHz	CT_{RT}			+70		dB
Idle noise, measured with 8 kHz sample and hold section (section connected to VFXO and gain setting op amp at unity gain)	N_{TO}	relative to 0.775 V_{rms}		−78.5	−77.5	dBm0p
				12	13	dBrnC0
		relative to a transmission level at +6 dBm, **see fig. 7**		−84.5	−83.5	dBm0p
				6	7	dBrnC0
Absolute delay at 1 kHz	D_{AX}			180	195	µs
Group delay distoration	D_{DX}					
500 Hz				200	250	µs
600 Hz				130	150	µs
1000 Hz				50	85	µs
2600 Hz				50	85	µs
2800 Hz				80	150	µs
Phase characteristic		(GSX to VFXO): inverting				

Receive filter						
Absolute passband gain at 1 kHz	G_{AR}	$R_L = \infty$	−0.1	0	+0.1	dB
Attenuation relative to 1 kHz with sin x/x correction	α_{RR}					
		0 dBm0				
0 to 3000 Hz		output signal =	−0.125		+0.125	dB
3400 Hz		1.55 V_{rms} at VFRO	−0.125	+0.2	+0.65	dB
3600 Hz			0			dB
4000 Hz			+14			dB
≧ 4600 Hz			+40			dB
Cross talk, attenuation transmit to receive	CT_{TR}			+70		dB
Idle noise measured at VFRO PWRO+ and PWRO− connected at unity gain	N_{RO}	relative to 0.775 V_{rms} **see fig. 8**		−78.5	−77.5	dBm0p
				12	13	dBrnC0
		relative to transmission level of + 6 dBm **see fig. 9**		−84.5	−83.5	dBm0p
				6	7	dBrnC0
Absolute dalay at 1 kHz	D_{AR}			130	140	µs
Group delay distortion	D_{DR}					
500 Hz				0	20	µs
600 Hz				0	20	µs
1000 Hz				5	50	µs
2600 Hz				85	100	µs
2800 Hz				110	150	µs
Phase characteristic		(VFRI to VFRO): inverting				

Figure 7

Test figure Transmit filter idle noise measurement

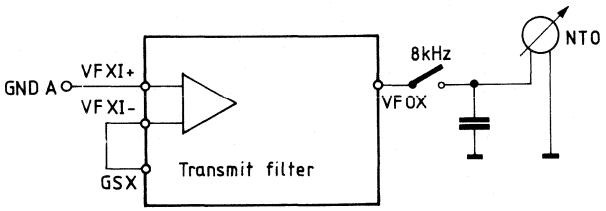


Figure 8

Test figure Receive filter idle noise measurement

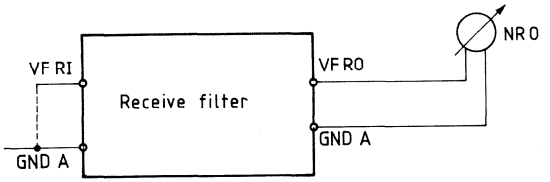
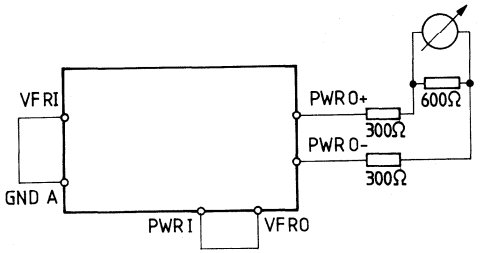


Figure 9

Test figure Receive filter idle noise measurement



Two-Channel PCM CODEC

SM 61 C

MOS circuit

Type	Ordering code	Package outline
SM 61 C	Q67100-Z140	DIC 28

Features

- Two-channel CODEC in one 28 pin package
- CCITT G 711 and G 732 compatible
- A-law or μ-law-companding possible, pin selectable
- 8 kHz sampling rate for two analog channels (16 kHz for one channel possible)
- Digital interface TTL-compatible (2.048 MHz- tristate-PCM output)
- On-chip temperature-compensated voltage reference
- Autozeroing
- ±5% power supplies: +12 V, +5 V, −5 V
- Total power consumption: 200 mW
  Standby power: 20 mW
- Cross talk suppression
- Simple control-logic; only one frame-synchronization pulse required

General description

The Siemens CODEC-system SM 61 C is a monolithic bipolar and an NMOS circuit; it codes and decodes signals in the voiceband range. The main application is in **P**ulse **C**ode **M**odulation (PCM 30/32) systems.

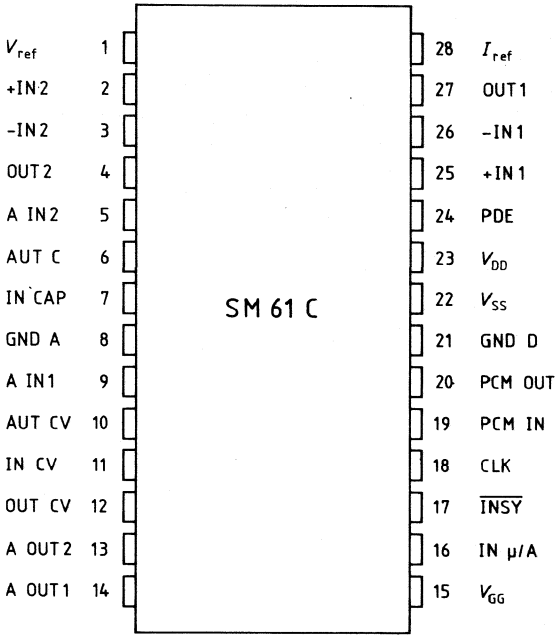
Designing the codec for two channels reduces the device count to one half per channel.

The NMOS-part contains the timing control, the input- and output-sampling circuits, the PCM register, the digital compressor and expander for A-law and μ-law, the D/A converter, the crosstalk suppression circuit and the autozero controls. The bipolar part contains the reference-current generator, the current-volltage converter, the comparator and two additional buffers (op amps).

A block diagram of a PCM system using the SM 61 C, is shown in **figure 1.**

Pin configuration

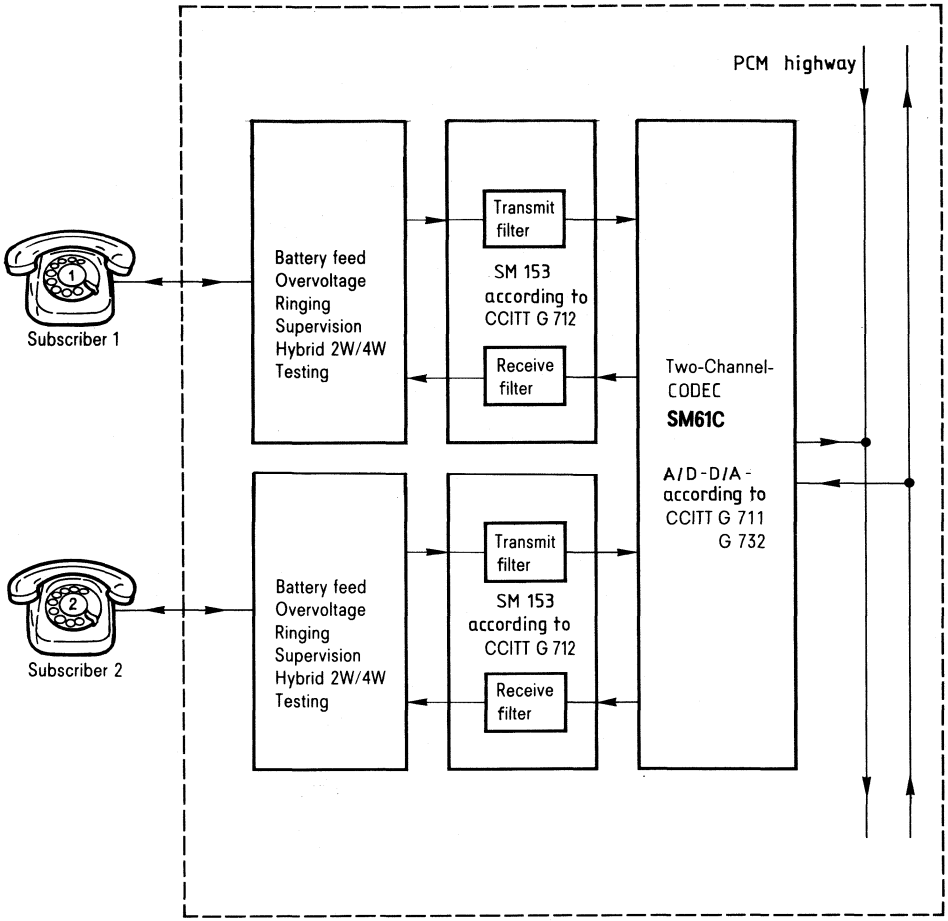
top view



Pin description

Pin No.	Symbol	Description
1	V_{ref}	Output of the reference voltage, ref = 1.25 V, temperature-compensated
2	+IN2	Non-inverting input } op amp2
3	−IN2	Inverting input } op amp2
4	OUT2	Output } op amp2
5	A IN2	Analog input for channel 2
6	AUT C	Connection for automatic zero capacitor C_2 (0.1 μF); compensates the comparator offset down to 0.1 mV
7	IN CAP	Connection for the input hold capacitor C_1 (2.2 nF, low impedance)
8	GND A	Analog ground, reference for all analog signals
9	A IN1	Analog input for channel 1
10	AUT CV	Connection for automatic zero capacitor C_3 (0.1 μF); compensates the current-voltage converter offset down to 0.1 mV
11	IN CV	Inverting input of current-voltage converter
12	OUT CV	Output of the current-voltage converter (can be discharged before automatic testing)
13	A OUT2	Analog output for channel 2 } (PAM signal)
14	A OUT1	Analog output for channel 1 } (PAM signal)
15	V_{GG}	Supply voltage +12 V ±5%
16	IN μ/A	Input for selecting the companding law; low-level = μ-law; high-level = A-law
17	$\overline{\text{INSY}}$	Input for the synchronizing pulse which controls the converter; duration at least one period of the 2.048 MHz clock; negative going edge synchronizes with internal time slot 0.
18	CLK	2.048 MHz clock = frequency of bit sequence, duty cycle 50%
19	PCM IN	Input from PCM highway serially at 2.048 MHz
20	PCM OUT	Output to PCM highway serially at 2.048 MHz
21	GND D	Digital ground; reference for all digital signals
22	V_{SS}	Supply voltage −5 V ±5%;
23	V_{DD}	Supply voltage +5 V ±5 %;
24	PDE	Power down enable; high level = power-down mode
25	+IN1	Non inverting input } op amp 1
26	−IN1	Inverting input } op amp 1
27	OUT1	Output } op amp 1
28	I_{ref}	Input of the reference current generator, resistor R_1 between V_{ref} and I_{ref} determines the reference current; recommended range for I_{ref} 180 μA < I_{ref} < 220 μA

Figure 1
PCM system block diagram



Functional description

Figure 2 shows the block diagram of the internal circuits of the Siemens CODEC and the necessary external connections. These are the sample and hold capacitor C_1, two autozero capacitors C_2, C_3 and two resistors R_1, R_2 which determine the output level.

Figure 2 and the timing diagram (**fig. 3**) are used as a basis for the following functional description of the CODEC.

In the **P**ulse **C**ode **M**odulation time multiplex system PCM 30/33 specified by CCITT, the bandwidth limited voice signals are sampled at 8 kHz.

The bitrate of PCM 30/32 is 2.048 Mbit/s, allowing time multiplexing of 30 voice and 2 signaling 8 bit PCM words. The coding of the analog signals into digital data and the corresponding decoding are performed according to nonlinear companding characteristics. This means that the analog to digital conversion is made by **compressing** from 13 bit to 8 bit code and the digital to analog conversion by a corresponding 8 bit to 13 bit linear code **expansion,** resulting in a signal to noise ratio improvement when considering the whole dynamic range.

The μ-and A-encoding laws are shown in **table 1a, 1b, 2a, 2b.** With the Siemens CODEC SM 61 C system the desired conversion law is pin-selectable.

The CODEC SM 61 C includes only one D/A converter with a temperature-compensated current reference, a current splitting $R/2$ R network and a current to voltage converter. This D/A converter, when combined with a comparator, a sampling capacitor and a succesive-approximation register, serves as the A/D converter as well.

Timing

The timing diagram (**fig. 3**) shows the coding of two subscribers during one frame of 125 μs.

The synchronization pulse $\overline{\text{INSY}}$ allocates the channel numbers of the subscribers on the PCM highway and starts the internal timing of the CODEC SM 61 C (time slot 0).

The PCM words for subscriber 1 are shifted in and out from the PCM highway during time slot 0 and for subscriber 2 during time slot 16.

The autozero-logic for the comparator and current-voltage converter compensates both offset voltages to less than 0.1 mV and suppresses any interface between the two channels.

The crosstalk suppression circuit forces the CODEC to transmit the zero code, if the last analog samples were smaller than the second-decision value.

Figure 2
Block diagram

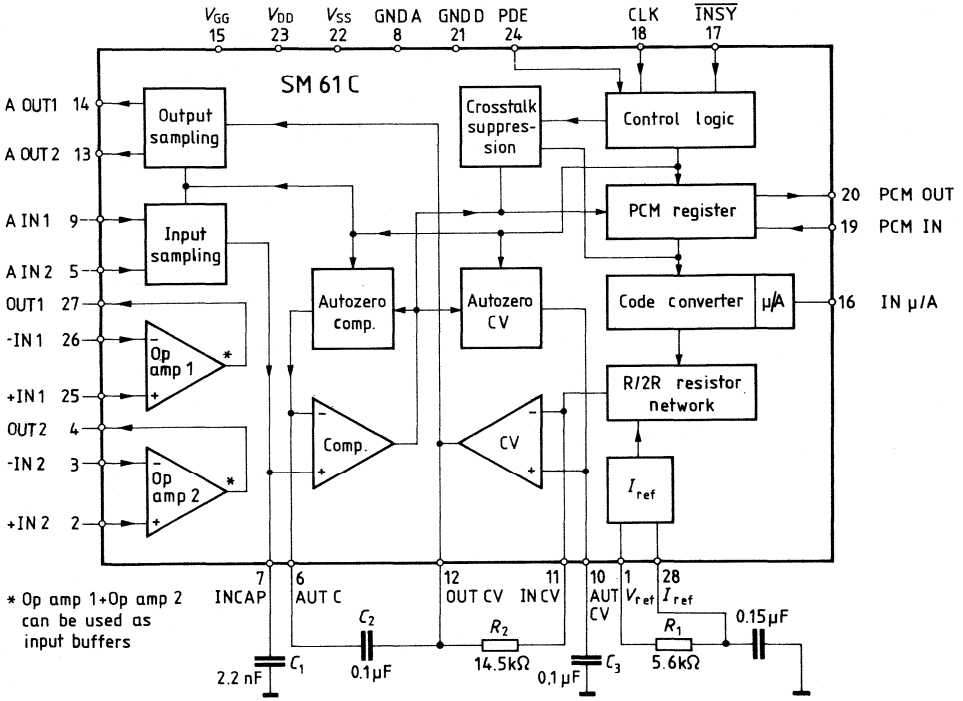


Figure 3
Timing diagram

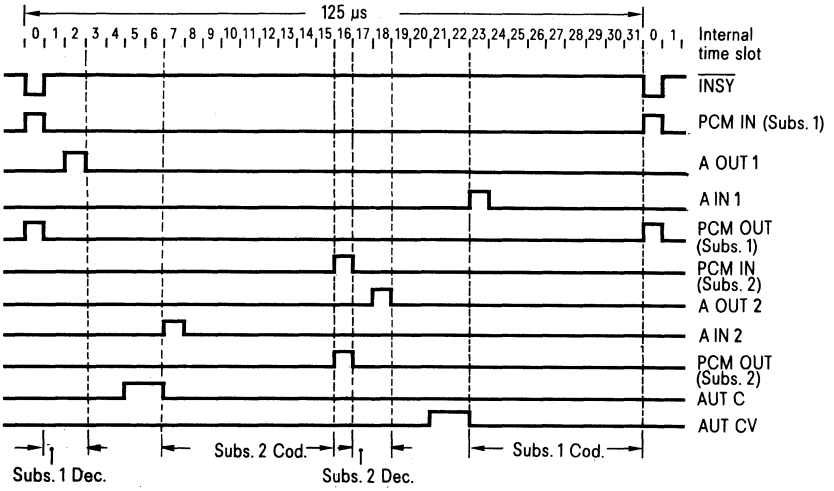


Table 1a

A-law: positive input values (CCITT G 711)

Segment number	Number of intervals x interval size	Value at segment end points	Decision value number n	Decision value x_n (1)	Character signal before inversion of the even bits Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (3)	Decoder output value number
		4096	(128)	(4096)			
			127	3968	1 1 1 1 1 1 1 1	4032	128
7	16 × 128				(2)		
			113	2176			
		2048	112	2048	1 1 1 1 0 0 0 0	2112	113
6	16 × 64				(2)		
			97	1088			
		1024	96	1024	1 1 1 0 0 0 0 0	1056	97
5	16 × 32				(2)		
			81	544			
		512	80	512	1 1 0 1 0 0 0 0	528	81
4	16 × 16				(2)		
			65	272			
		256	64	256	1 1 0 0 0 0 0 0	264	65
3	16 × 8				(2)		
			49	136			
		128	48	128	1 0 1 1 0 0 0 0	132	49
2	16 × 4				(2)		
			33	68			
		64	32	64	1 0 1 0 0 0 0 0	66	33
1	32 × 2				(2)		
			1	2			
↓			0	0	1 0 0 0 0 0 0 0	1	1

Notes:
1): 4096 normalized value units correspond to T_{max} = 3.14 dBm0
2): The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to positive input values between two successive decision values numbered n+1 (see column 4) is (128+n) expressed as a binary number.
3): The value at the decoder output is $y_n = \frac{x_{n-1} + x_n}{2}$ for n = 1,.... 127, 128
4): x_{128} is a virtual decision value

Table 1b

A-law: negative input values (CCITT G 711)

Segment number	Number of intervals x interval size	Value at segment end points	Decision value number n	Decision value x_n (1)	Character signal before inversion of the even bits Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (3)	Decoder output value number
↑			0	0			
			1	−2	0 0 0 0 0 0 0 0	− 1	1
1	32 × 2				(2)		
		−64	32	−64			
			33	−68	0 0 1 0 0 0 0 0	− 66	33
2	16 × 4				(2)		
		−128	48	−128			
			49	−136	0 0 1 1 0 0 0 0	− 132	49
3	16 × 8				(2)		
		−256	64	−256			
			65	−272	0 1 0 0 0 0 0 0	− 264	65
4	16 × 16				(2)		
		−512	80	−512			
			81	−544	0 1 0 1 0 0 0 0	− 528	81
5	16 × 32				(2)		
		−1024	96	−1024			
			97	−1088	0 1 1 0 0 0 0 0	−1056	97
6	16 × 64				(2)		
		−2048	112	−2048			
			113	−2176	0 1 1 1 0 0 0 0	−2112	113
7	16 × 128				(2)		
			127	−3968			
		−4096	(128)	(−4096)	0 1 1 1 1 1 1 1	−4032	128

Notes:
1): 4096 normalized value units correspond to $T_{max} = 3.14$ dBm0
2): The character signals are obtained by inverting the even bits of the signals of column 6. Before this inversion, the character signal corresponding to negative input values between two successive decision values numbered n+1 (see column 4) is (128+n) expressed as a binary number.
3): The value at the decoder output is $y_n = \frac{x_{n-1} + x_n}{2}$ for n = 1,.... 127, 128
4): x_{128} is a virtual decision value

Table 2a

μ-law: positive input values (CCITT G 711)

Segment number	Number of intervals x interval size	Value at segment end points	Decision value number n	Decision value x_n (1)	Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (3)	Decoder output value number
		8159	(128)	(8159)			
					1 0 0 0 0 0 0 0	8031	127
			127	7903			
8	16 × 256				(2)		
			113	4319			
		4063			1 0 0 0 1 1 1 1	4191	112
			112	4063			
7	16 × 128				(2)		
			97	2143			
					1 0 0 1 1 1 1 1	2079	95
		2015	96	2015			
6	16 × 64				(2)		
			81	1055			
					1 0 1 0 1 1 1 1	1023	80
		991	80	991			
5	16 × 32				(2)		
			65	511			
					1 0 1 1 1 1 1 1	495	64
		479	64	479			
4	16 × 16				(2)		
			49	239			
					1 1 0 0 1 1 1 1	231	48
		223	48	223			
3	16 × 8				(2)		
			33	103			
					1 1 0 1 1 1 1 1	99	32
		95	32	95			
2	16 × 4				(2)		
			17	35			
					1 1 1 0 1 1 1 1	33	16
		31	16	31			
1	15 × 2				(2)		
			2	3			
					1 1 1 1 1 1 1 0	2	1
↓	1 × 1		1	1	1 1 1 1 1 1 1 1		
			0	0		0	0

Notes: 1): 8159 normalized value units correspond to $T_{max} = 3.17$ dBm0

2): The character signal corresponding to positive input values between two succesive decision values numbered n and n+1 (see column 4) is (255−n) expressed as a binary number.

3): The value at the decoder output is $y_o = x_o = 0$ for $n = 0$ and $y_n = \frac{x_n + x_n + 1}{2}$ for $n = 1, 2, \ldots . 127$

4): x_{128} is a virtual decision value

Table 2b

μ-law: negative input values (CCITT G 711)

Segment number	Number of intervals x interval size	Value at segment end points	Decision value number n	Decision value x_n (1)	Bit number 1 2 3 4 5 6 7 8	Value at decoder output y_n (3)	Decoder output value number
↑			0	0		0	0
	1 × 1		1	−1	0 1 1 1 1 1 1 1		
1			2	−3	0 1 1 1 1 1 1 0	− − 2	1
	15 × 2		⋮	⋮	⋮ (2)	⋮	⋮
		−31	16	−31			
			17	−35	0 1 1 0 1 1 1 1	− − 33	16
2	16 × 4		⋮	⋮	⋮ (2)	⋮	⋮
		−95	32	−95			
			33	−103	0 1 0 1 1 1 1 1	− − 99	32
3	16 × 8		⋮	⋮	⋮ (2)	⋮	⋮
		−223	48	−223			
			49	−239	0 1 0 0 1 1 1 1	− −231	48
4	16 × 16		⋮	⋮	⋮ (2)	⋮	⋮
		−479	64	−479			
			65	−511	0 0 1 1 1 1 1 1	− −495	64
5	16 × 32		⋮	⋮	⋮ (2)	⋮	⋮
		−991	80	−991			
			81	−1055	0 0 1 0 1 1 1 1	−1023	80
6	16 × 64		⋮	⋮	⋮ (2)	⋮	⋮
		−2015	95	−2015			
			97	−2143	0 0 0 1 1 1 1 1	−2079	96
7	16 × 128		⋮	⋮	⋮ (2)	⋮	⋮
		−4063	112	−4063			
			113	−4318	0 0 0 0 1 1 1 1	−4191	112
8	16 × 256		⋮	⋮	⋮ (2)	⋮	⋮
			126	−7647			
			127	−7903	0 0 0 0 0 0 0 1	−7775	126
		−8159	(128)	(−8159)	0 0 0 0 0 0 0 0	−8031	127

Notes: 1): 8159 normalized value units correspond to T_{max} = 3.17 dBm0

2): The character signal corresponding to negative input values between two successive decision values numbered n and n+1 (see column 4) is (127−n) expressed as a binary number for n = 0.1, ... 127.

3): The value at the decoder output is $y_o = x_o = 0$ for n = 0 and $y_n = \frac{x_n + x_{n+1}}{2}$ for n = 1, 2, ... 127

4): x_{128} is a virtual decision value

Maximum ratings

		Min.	Max.	Unit
Supply voltage (relative to GND D)	V_{GG}	−0.3	15	V
	V_{DD}	−0.3	10	V
	V_{SS}	−10	0	V
Output current of op amps (op amp 1, op amp 2, CV)	I_O	−30	30	mA
Differential input voltage of op amps	V_I	−8	8	V
Input voltage of op amps and comparator (relative to GND A)	V_I	V_{SS}	V_{DD}	V
Input voltage digital	V_{ID}	−0.3	18	V
Output voltage digital	V_{OD}	−0.3	18	V
Input voltage digital PDE	V_{PDE}	−0.3	8	V
Operating temperature	T_{amb}	−25	75	°C
Storage temperature	T_{stg}	−55	125	°C
Junction temperature	T_j		125	°C
Thermal resistance (junction to ambient)	R_{thJA}		50	K/W
Total power dissipation	P_{tot}		600	mW

Operating characteristics

(V_{SS}= −5V ±5%, V_{DD} = +5V ±5%, V_{GG} = 12V ±5%, f_{CL} = 2.048 MHz, T_{amb} = 0 to 70°C)

Power dissipation		Test conditions	Min.	Typ.	Max.	Unit
Standby current	I_{GGO}		0	1.5	3	mA
Standby current	I_{DDO}		0	100	200	µA
Standby current	I_{SSO}		−1.7	−1.0	0	mA
Operating current	I_{GGI}		7	10	16	mA
Operating current	I_{DDI}		4	6	10	mA
Operating current	I_{SSI}		−11	−7	−6	mA

Operating characteristics

($V_{SS} = -5\,V \pm 5\%$, $V_{DD} = +5\,V \pm 5\%$, $V_{GG} = 12\,V \pm 5\%$, $f_{CL} = 2.048$ MHz, $T_{amb} = 0$ to 70°C)

Digital interface		Test conditions	Min.	Typ.	Max.	Unit
L input voltage (CLK, INμ/A, $\overline{INSY}$, PCM, IN, PDE)	V_{IL}				0.8	V
H input voltage	V_{IH}		2.0		V_{DD}	V
L output voltage	V_{OL}	$I_{OL} = 2$ mA	0	0.2	0.4	V
H output voltage	V_{OH}	$I_{OL} = 0.2$ mA	3.5		V_{DD}	V
Input capacitance (CLK, $\overline{INSY}$, PCM IN)	C_I	$V_I = 5\,V$, $f = 1$MHz		2		pF
Input capacitance (PDE, INμ/A)	C_I	$V_I = 5\,V$, $f = 1$ MHz		5		pF
Input current (PDE, INμ/A)						
L level	I_{IL}	$V_{IL} = 0$ V	−100			μA
H level	I_{IH}	$V_{IH} = V_{DD}$			1	μA
Input current (CLK, $\overline{INSY}$, PCM, IN)						
L level	I_{IL}	$V_{IL} = 0$ V			1	μA
H level	I_{IH}	$V_{IH} = V_{DD}$			1	μA

Subscriber analog interface						
Resistance of samplers (A IN1, A IN2, A OUT1, A OUT2)	R_{ON} R_{OFF}		50 200	150	200	Ω MΩ
Input voltage range (A IN1, A IN2)	V_I		$V_{SS}+1.5$		$V_{DD}-1.0$	V
Acquisition time (A IN1, A IN2, A OUT2)	t_{Aq}			3.9	3.9	μs
Output voltage (A OUT1, A OUT2)	V_O	PAM signal with 3.9 μs pulse-width	$V_{SS}+1.8$		$V_{DD}-1.8$	V

Analog interfaces Reference current generator (I_{ref}, V_{ref})						
Reference voltage	V_{ref}		1.2	1.25	1.3	V
Temperature coefficient of V_{ref}	TC		−200	0	250	$ppmK^{-1}$
Input offset voltage	$V_{I\,ref}$		0	13	20	mV

Comparator						
Input bias current	$I_{IN\,CAP}$, I_{AUTC}				30	nA
Remaining input offset voltage (compensated by autozero)	$V_{IN\,CAP}$, V_{AUTC}		−0.1		0.1	mV
Input common mode range	$V_{IN\,CAP}$, V_{AUTC}		$V_{SS}+1.5$		$V_{DD}-1.0$	V

Operational amplifier current voltage converter

		Test conditions	Min.	Typ.	Max.	Unit
Input bias current (+IN1, −IN1, +IN2, −IN2, IN CV, AUT CV)	I_I			10	30	nA
Input offset current (+IN1, −IN1, +IN2, −IN2)	$+I_{OS}$ $-I_{OS}$				10	nA
Input offset voltage (+IN1, −IN1, +IN2, −IN2)	$+V_{OS}$ $-V_{OS}$		−10		10	mV
Remaining input offset voltage (IN CV) compensated by autozero	$V_{IN\,CV}$ $-V_{GND\,A}$		−0.1		0.1	mV
Input common mode range (+IN1, −IN1, +IN2, −IN2)	$+V_I$ $-V_I$		$V_{SS}+1.5$		$V_{DD}-1.0$	V
Voltage gain (op amp 1, op amp 2, CV)	G_V		60	75		dB
Output voltage range	V_{O1}, V_{O2} $V_{O\,CV}$		$V_{SS}+1.8$		$V_{DD}-1.8$	V
Output current	I_O		−20		20	mA
Slew rate	dV_O/dt			2		V/µs
Settling time (OUT1, OUT2, OUT CV)	t_s	settling time (1%) $G_V = 1$		0.5		µs

Timing specification (fig. 4)

Clock	CLK			2.048		MHz
Clock period	t_{CLY}			488.3		ns
Clock rise and fall time	t_r, t_f				20	ns

Synchronizing pulse input $\overline{INSY}$

Delay time	t_{SYD}			50		ns
L pulse width	t_{WL}		0.5		124	µs

PCM IN

New data setup	t_{DS}		100	150		ns
Hold time	t_H		50			ns

PCM OUT

Delay time	t_D			100	150	ns
Rise time	t_{TLH}	200 pF load			100	ns
Fall time	t_{THL}	200 pF load			100	ns

System characteristic (half-channel conditions)

		Test conditions		Min.	Max.	Unit
Gain tracking encoder	ΔG	−40 dBm0	input level	−0.3	+0.25	dB
		−50 dBm0		−0.55	+0.5	dB
		for other values see **figure 5**				
Gain tracking decoder	ΔG	−40 dBm0	input level	−0.25	+0.3	dB
		−50 dBm0		−0.5	+0.55	dB
		for other values see **figure 5**				

		Encoder	Decoder	
Signal-to-total distortion	S/D	**figure 6**	**figure 7**	
Idle channel noise	N_{IC}	max. −67.4	max. −77.6	dBm 0p
		typ. −95	typ. −85	dBm 0p
Cross talk (f = 0.3–3.4 kHz)		max. −70		dBm 0
between the two channels		typ. −76		dBm 0
between the two decoders		max. −76		dBm 0
		typ. −80		dBm 0

		Min.	Typ.	Max.	
Input level (at $I1$, $I2$) corresponding to 0 dBm 0	G_I	5.95	6.05	6.15	dBm [1]
Digital milliwatt response at approx. 800 Hz DmW (at 1000 Hz according to CCITT G 711 requires sin x/x correction)		5.59	5.69	5.79	dBm [2]
Load dependence of outputs A OUT1, A OUT2			**figure 9**		

[1] Using external reference voltage of 2.49 V and 1 MΩ load, selective measurement at A OUT1, A OUT2 **fig. 8.**

[2] Using coupling capacitor 0.15 µF and external reference stage of 2.49V, f = 814 Hz **fig. 8.**

[1] [2] T_{amb} = 25°C, AOL = 2.5

Figure 4

Timing diagram

Clock (CLK), Synchronization ($\overline{INSY}$), PCM IN and PCM OUT

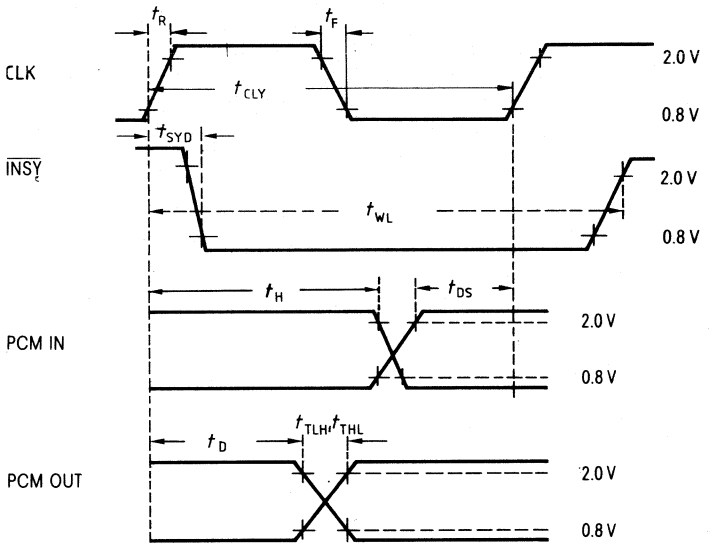
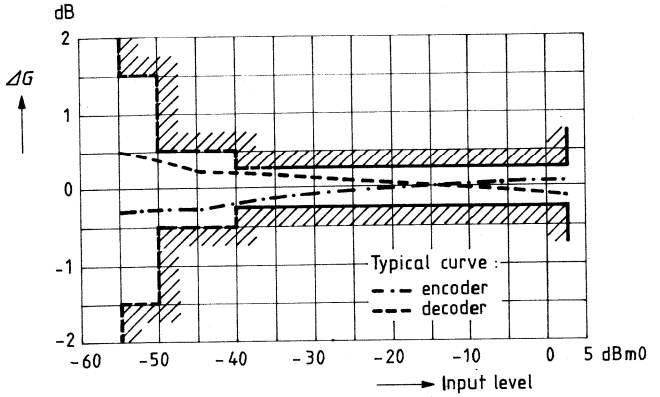


Figure 5

Gain tracking Δ G for encoder and decoder [1)]

(sine wave measurement with 814 Hz)



1) Values for −40 dBm0 and −50 dBm0 see gain tracking: page 150

Figure 6

Signal-to-total distortion *S/D* for encoder
(level −3 dBm0 to −45 dBm0 with band-limited noise, level <−45 dBm0 with sine wave)

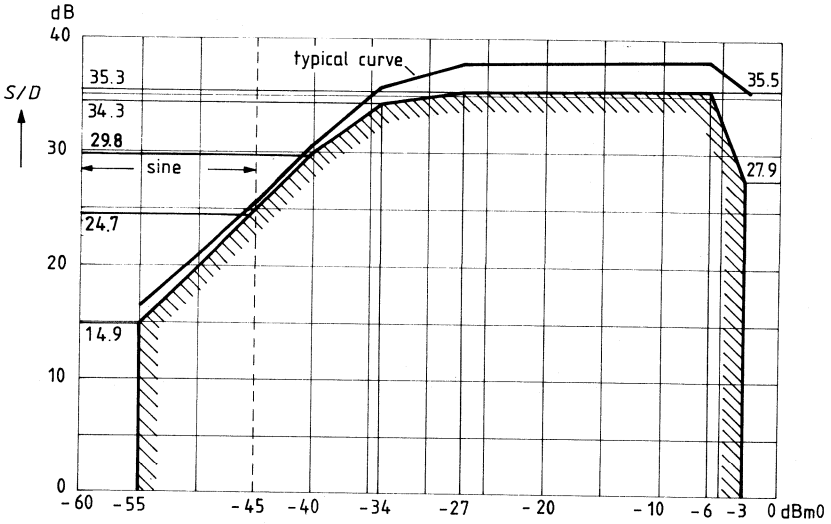


Figure 7

Signal-to-total distortion *S/D* for decoder
Measured with band-limited noise

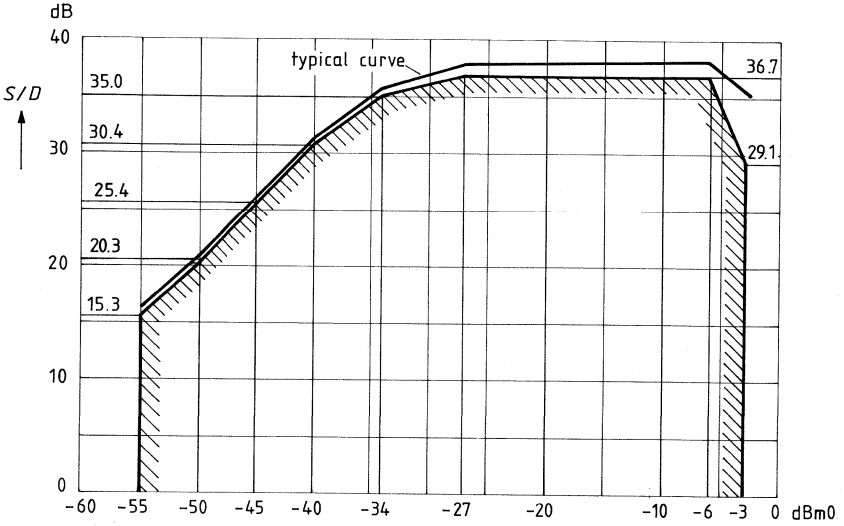


Figure 8

Schematic diagram for measurement of nominal levels

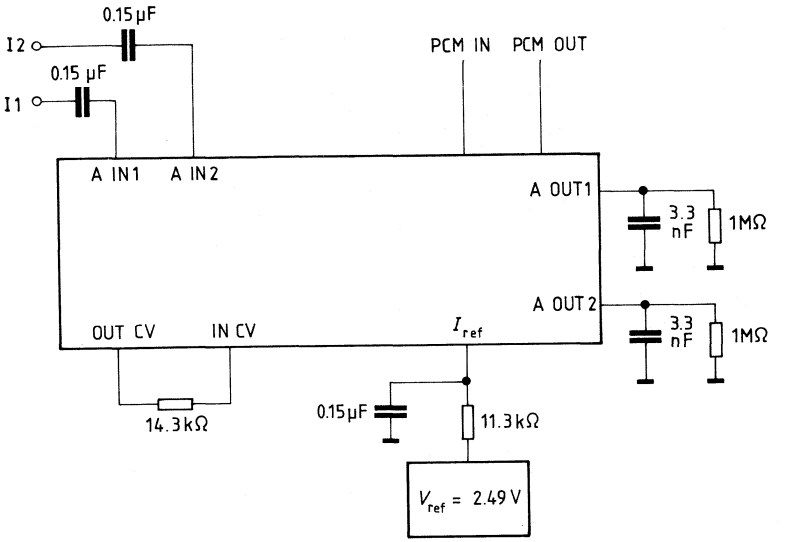


Figure 9

Load dependence of outputs A OUT 1, A OUT 2

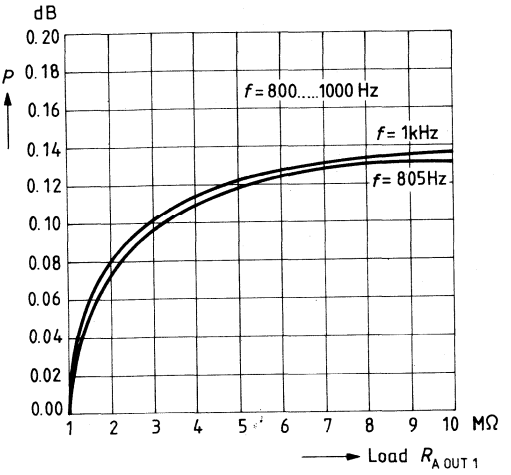
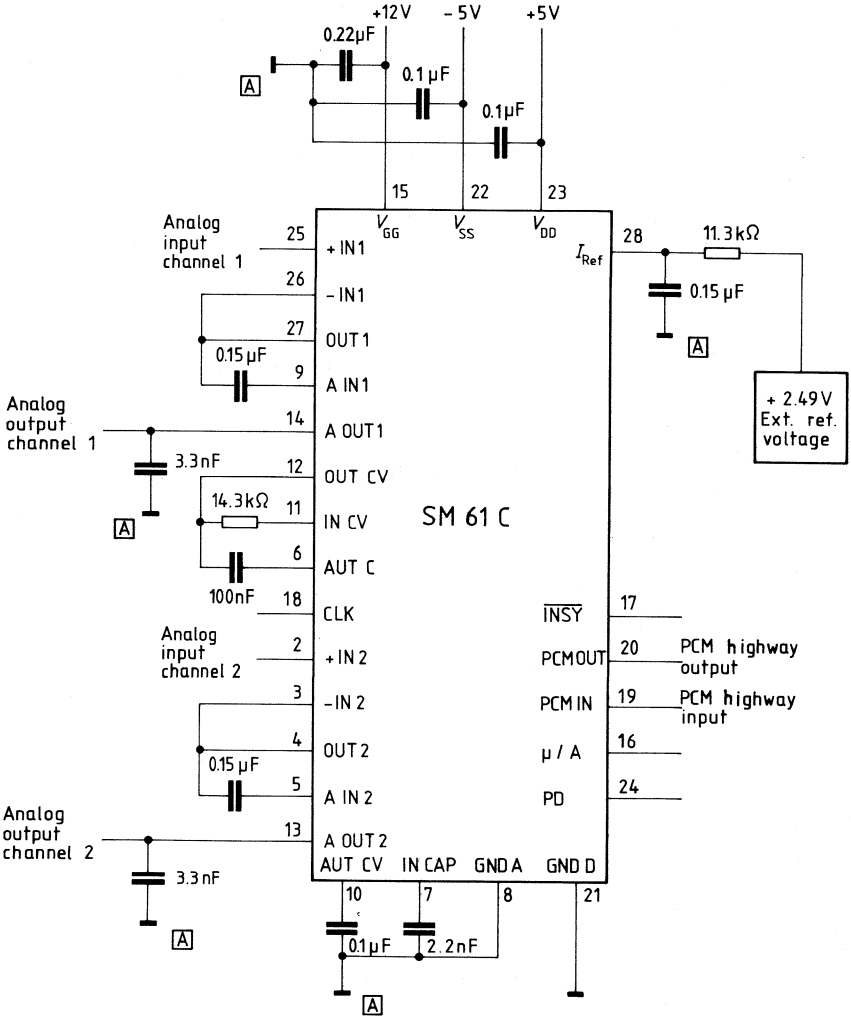


Figure 10
Typical application



Frame Aligner Module

PEB 2030 (SM 300 B)

Preliminary data

MOS circuit

Type	Ordering code	Package outline
PEB 2030	Q 67100–Y 785	DIC 24

Features

- Detection of frame alignment signals for PCM 30 highways in accordance with CCITT recommendation G 732
- Delay compensation and clock alignment between transmission line and exchange
- Compensation of phase jitter up to 60 µs
- Detection and initiation of route alarms (AIS, service word)
- Indication of loss of frame alignment
- Slip detection
- Error simulation for test purposes
- Digital interface TTL-compatible

Applications

The PEB 2030 frame aligner module is used for interfacing PCM 30 routes with PCM switching networks.
Its main applications are as follows:

- In multiplex units for PCM transmission routes
- In concentrators and subscriber multiplexers at one end of PCM routes
- As an interface between PCM routes and public and private PCM switches (DIU)
- For delay compensation between switching stages (e.g. Swiss Post Office IFS design concept)

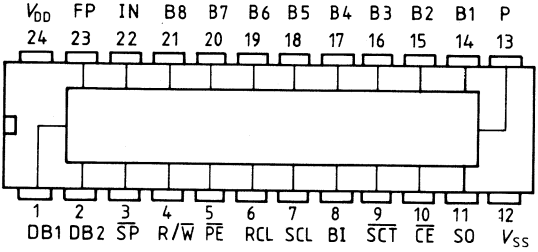
General description

The Siemens frame aligner module PEB 2030 is a monolithic NMOS circuit. Its main application is detection of frame alignment signals of PCM 30 routes according to CCITT recommendation G 732 and the clock adjustment with delay compensation between PCM routes and PCM switches.

An incorporated buffer enables the PEB 2030 to compensate phase jitter up to 60 µs. Route alarms can be challenged by a bidirectional data interface.

Pin configuration

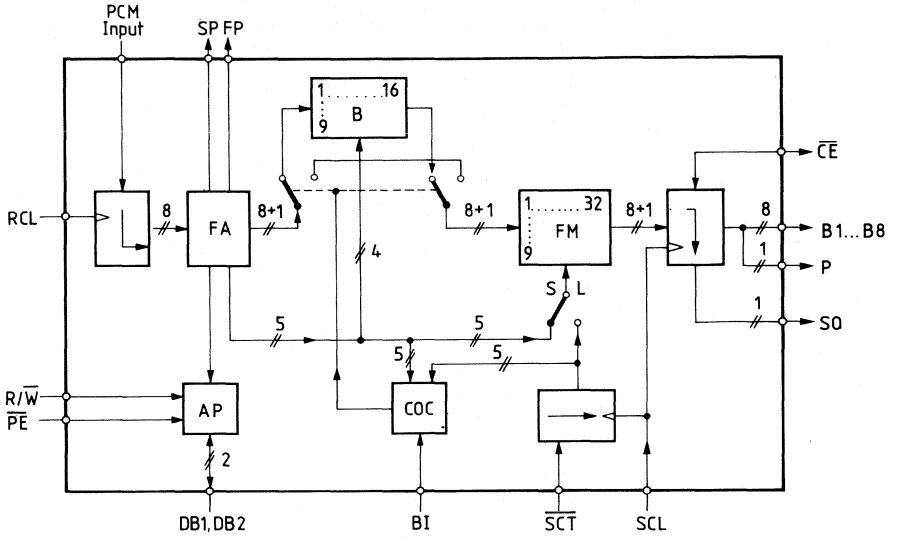
top view



Pin designation

Pin No.	Symbol	Description
1	DB 1	Data interfaces
2	DB 2	
3	$\overline{SP}$	Synchronous pulse
4	R/$\overline{W}$	Direction of data transfer
5	$\overline{PE}$	Alarm port enable
6	RCL	Route clock
7	SCL	Station clock
8	BI	Buffer inactive
9	$\overline{SCT}$	Station counter trigger pulse
10	$\overline{CE}$	Chip enable
11	SO	Serial output
23	FP	Fault pulse
22	IN	PCM input
14	B 1	Parallel outputs
.	.	
.	.	
.	.	
21	B 8	
13	P	Parity bit
12	V_{SS}	Ground (0 V)
24	V_{DD}	Supply voltage (+5 V)

Block diagram



FA Frame alignment
AP Alarm port
B Buffer
COC Coincidence circuit
FM Frame memory

Functional description

The PEB 2030 module is fabricated using the n-channel depletion technology.

The module, connected to a PCM 30 line, and the associated input clock (route clock RCL), are synchronized with the PCM frame in accordance with CCITT recommendation G 732. In the stable condition the module supplies 488 ns synchronous pulses ($\overline{SP}$) at a bit rate of 4 Kbits/s which identify the beginning of the PCM frames containing the bunched frame alignment signal (FAS). During the synchronizing phase and in the event of frame alignment being lost, the synchronizing pulses are are suppressed and a 2 µs fault pulse FP is delivered every 250 µs. When a synchronized state exists, such a fault pulse appears only if an FAS is not recognized.

On the output side the PCM information can be read out in serial and in parallel form. For this purpose, a reading clock (SCL) and a 488 ns reading synchronizing pulse ($\overline{SCT}$) must be applied at 250 µs intervals to fix the beginning of the frame. The module supplies a parity check bit (even parity) to each PCM word via a tri-state output which is activated by a chip enable ($\overline{CE}$) in the same way as the tri-state outputs for the parallel information.

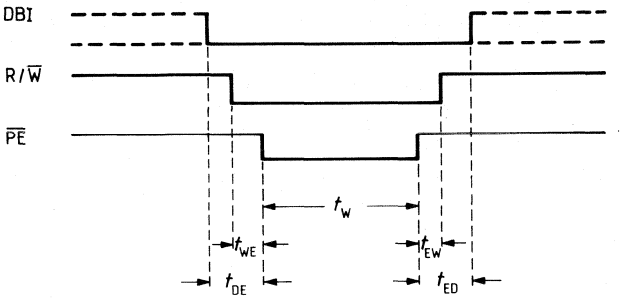
An alarm flipflop (FA Alarm) in the module is set in the event of frame alignment loss, route timing loss or loss the $\overline{CE}$ or $\overline{SCT}$ signals. The alarm bit is recorded in another flipflop in the service word (bit 3), whereas a third flipflop stage is set when logic '1' signals are received by the PCM route for the duration of two frames (Alarm Indication Signal AIS). A further flipflop is set when a slip of the frame occurs. The alarms are polled via a bidirectional data interface. The alarm circuits can be triggered and reset for test purposes via the data interface.

Pin description

Symbol	Function	Description
1. Supply		
V_{DD} V_{SS}	+5V ±5% 0 V	Power consumption 300 mW
2. PCM interfaces		
IN	PCM input	Information bit from one negative RCL edge to the next.
RCL	2.048 MHz ±50 ppm	Route clock
B1 ... B8	256 Kbit/s	Parallel PCM output information B1 = most significant inf. bit
P	256 Kbit/s	Parity bit (even parity)
SO	2.048 Mbit	Serial PCM output. Bit sequence with decreasing significance.
SCL	2.048 MHz	Station clock. Information bits from one neg. SCL edge to the next.
3. Control signals		
$\overline{SCT}$	4 Kbit/s width 488 ns	From one neg. SCL edge to the next. Frame begins at pos. $\overline{SCT}$ edge.
$\overline{SP}$	4 Kbit/s width 488 ns	From one neg. RCL edge to the next. Frame begins with FAS at pos. $\overline{SP}$ edge.
BI	Continuous signal	BI = 1 or not connected: Buffer inactive
FP	Width: 4×488 ns = 1.95 µs	Fault pulse delivered for every undetected FAS or every 250 µs in the event of frame alignment loss.
$\overline{CE}$	256 Kbit, with 488 ns or continuous level	Chip enable controls outputs B1 to B8, P low-impedance. The $\overline{CE}$ must be active during the $\overline{SCT}$, so that the $\overline{SCT}$ supervision by station counter is not impaired.

4. Data interface

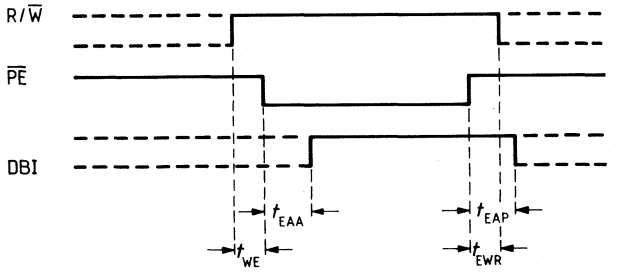
Write



DBI input timing (Write)

$t_W > 1\ \mu s$
$t_{WE} > 100$ ns
$t_{DE} > 100$ ns
$t_{EW} > 50$ ns
$t_{ED} > 150$ ns

Read



DBI output timing (Read)

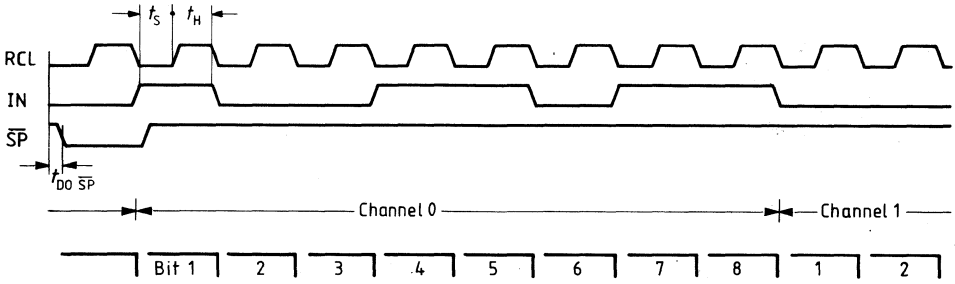
$t_{EWR} > 100$ ns
$0.8 < t_{EAA} < 1.2\ \mu s$
$C_L = 300$ pF
$t_{EAP} > 160$ ns
$t_{WE} > 100$ ns

Data transfer direction
R/$\overline{W}$ = 1 read alarm port
R/$\overline{W}$ = 0 write alarm port
Alarm port enable
bidirectional data interface for command acceptance or alarm signaling:

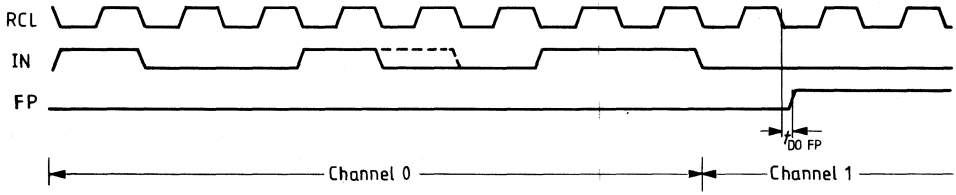
DB2	DB1
0	0 Command: poll FA alarm, AIS alarm
0	1 Command: poll B3 of the service word, Slip alarm
1	0 Command: reset alarm flipflop
1	1 Command: failure simulation
AIS alarm	FA alarm
Slip alarm	B3 alarm
	Alarms are signaled as log. '1'

Pulse diagram

Delivery of synchronous pulse $\overline{SP}$ in synchronized state

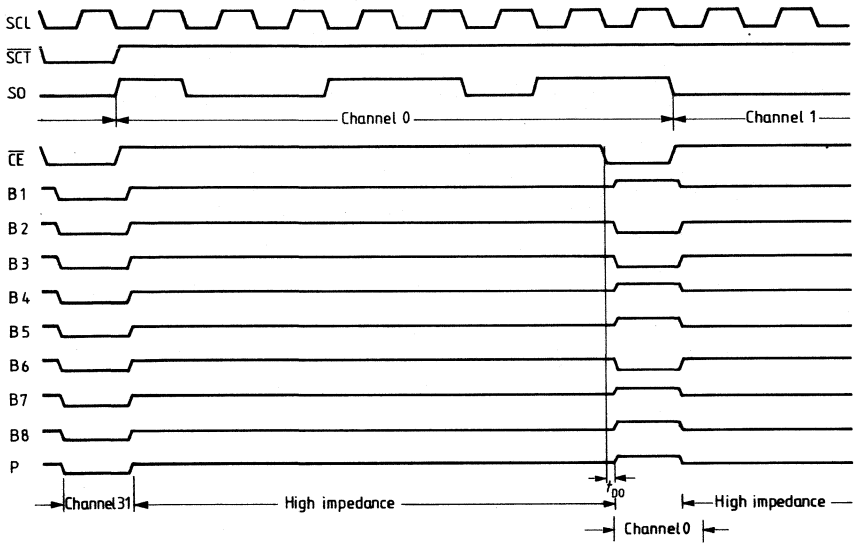


Delivery of fault pulse FP in the event of erroneous frame alignment signal

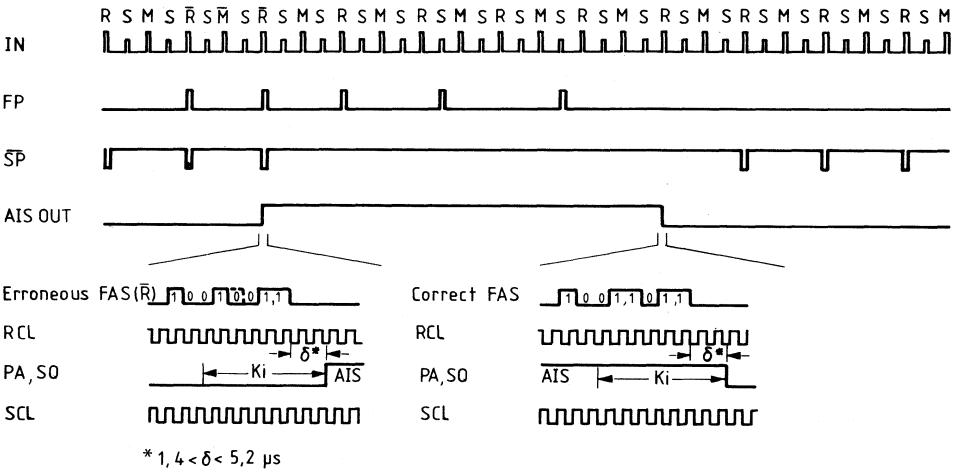


Pulse diagram

Output signals (B1 to B8, P) as functions of the station trigger pulse $\overline{SCT}$ and chip enable $\overline{CE}$



Loss of frame alignment due to bit falsification on the PCM route



R	Frame alignment signal (FAS)
M	Service word
S	Simultated FAS (Random FAS)
$\overline{R}$	Erroneous FAS
$\overline{M}$	Erroneous service word

Maximum ratings

		Min.	Max.	Unit
Input voltage	V_I	−0.3	7	V
Supply voltage	V_{DD}	−0.3	7	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	−55	125	°C
Total power consumption	P_{tot}		400	mW

Electrical characteristics (T_{amb} = 25°C)

		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Supply current	I_S		50	70	mA
Input current	I_{IL}	50		150	µA
H input voltage	V_{IH}	2.4			V
L input voltage	V_{IL}			0.7	V
L output voltage	V_{OL}			0.4	V
H output voltage	V_{OH}	2.7			V
H output current (FP, SO, SP, BI, P)	I_{OH}			−0.02	mA
L output current (FP, SO, SP, BI, P)	I_{OL}			0.46	mA
H output current (DBi)	I_{OH}			−0.04	mA
L output current (DBi)	I_{OL}			0.9	mA

Timing specification

Input H−L transfer time	t_{HL}			20	ns
Input L−H transfer time	t_{LH}			20	ns
Clock frequency (pulse-pause ratio 1 : 1) $t_{WH} : t_{WL}$	f_{CL}	0.2	2.048 1	2.1	MHz
Setup time	t_S	150			ns
Hold time	t_H	40			ns

Switching times (V_{DD} = 5 V, T_{amb} = 25°C)

from (input)	to (output)		Test conditions	Min.	Typ.	Max.	Unit
$\overline{CE}$	B1 ... B8, P	t_{DO}	50 pF, 10 kΩ			200	ns
SCL	DB1, DB2	t_{DO}	50 pF, 5kΩ			350	ns
RCL	FP, SP	t_{DO}	15 pF, 10 kΩ			200	ns
SCL	SO	t_{DO}	15 pF, 10 kΩ			200	ns

Decoder for Dual-Tone Multiple Frequency (DTMF) Receiver

SM 301 A4

Preliminary data **MOS circuit**

Type	Ordering code	Package outline
SM 301 A4	Q 67100–X 301–S 20	DIC 24

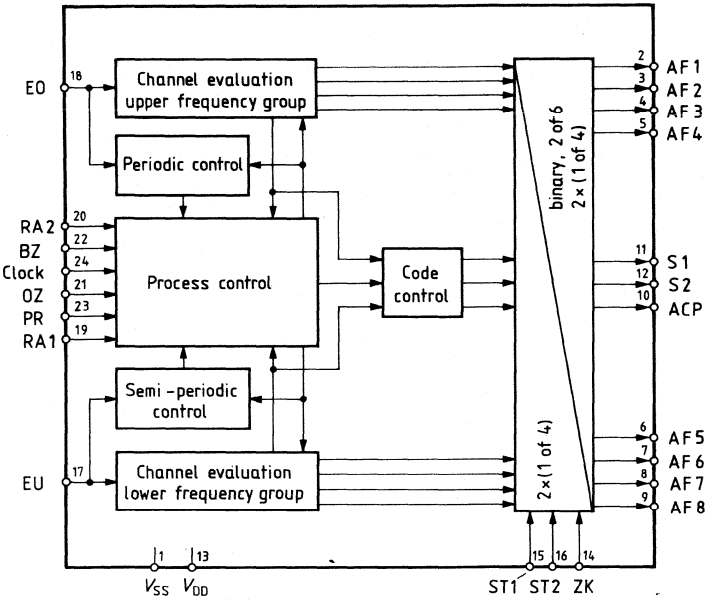
The decoder SM 301 A4 is used as the digital section for dual-tone MF pushbutton dialing with speech guarding in telephone switching systems. It processes pushbutton dialing signals in 2× (1-out-of-4) code according to CCITT recommendation Q 23 with or without accompanying DC signals.
The square-wave voltage signals are converted to DC signals. Hence, there are three output codes to choose from. A preceding analog section completely separates the two-tone frequency groups by means of filters (minimum stopband attenuation a_S = 27 dB), blocks the dialing tone (minimum stopband attenuation a_S = 40 dB), converts the now separated tone frequencies to digitally, evaluable square-wave signals and provides for supplementary speech guarding measures.

Features

- Technology: n-channel silicon-gate with depletion transistors
- CEPT specification fulfilled
- High speech guarding
- High immunity to interference (choice of either 12 dB or 4 dB signal/noise ratio)
- Economical standard clock crystal (2^{22} Hz)
- Digital evaluation of dual-tone MF signals and conversion to different output codes with scanning
  - 2×(1-out-of-4) code
  - Binary code
  - 2-out-of-6 code

  } 16 combinations with carry
- Code checking output for information acceptance
- Suitability for dual-tone MF dialing techniques (according to CEPT)
  - without accompanying DC signals
  - with accompanying DC signals
- Typical evaluation period
  - without accompanying DC signals: 28 ms
  - with accompanying DC signals: 15 ms (12 to 19 ms)
- 2 splitting outputs for quick separation of the continuing speech path even with high noise levels
  - typical response time of the splitting outputs:
  - S1: typ. 3 ms
  - S2: typ. 15 ms (12 to 19 ms)
- Holding time of the signal output freely selectable by means of appropriate connection.
  - Constant holding time for the bridging of signal interruptions ≦ 20 ms at the input of the complete dual-tone MF receiver according to CEPT.
  - Freely selectable holding time with external timing circuit.
  - No holding time for higher transmission speeds up to 20 signals per second.
- Simple matching of different output interfaces.
  - Electronic interface for the circuit types TTL, CMOS, NMOS
  - Relay drive with 2 mA input current
- Low power consumption (typ. 80 mW)
- 5 V power supply

Block diagram

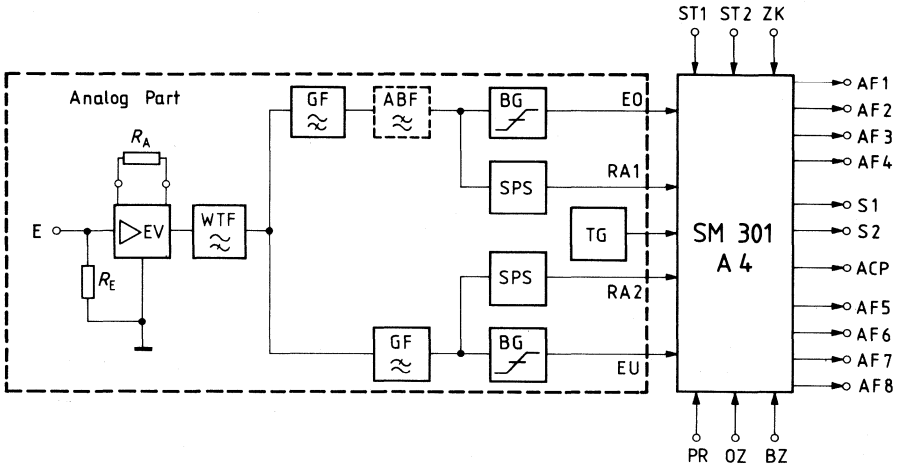


Pin designation

Pin No.	Symbol	Description
18, 17	EO, EU	Inputs – upper or lower frequency group
19, 20	RA1, RA2	Inputs for access to the speech guard circuits
15, 16	ST1, ST2	Control inputs for output code with pullup resistors
14	ZK	Control input for external control of the release time with pullup resistor
22	BZ	Control input for the accompanying of signal technique
21	OZ	Control input for changeover of output time extension
23	PR	Control input for switching of *S/N* ratio 12 dB / 4 dB
2 ... 9	AF1, ... AF8	Signal outputs
10	ACP	Code checking output (delayed by about 0.5 µs relative to AF1 to AF8)
11, 12	S1, S2	Splitting outputs
1	V_{SS}	Ground
13	V_{DD}	Supply voltage (+5 V)

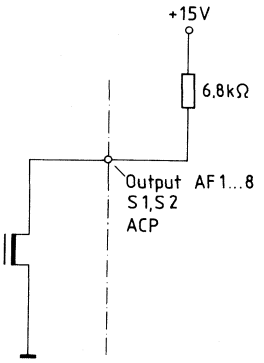
Application

A typical example of complete pushbutton dialing receiver with SM 301 A4



E	Input
EV	Input amplifier
WTF	Dialing tone filter
GF	Group filter
ABF	Outband filter
BG	Limiter
SPS	Speech guard circuit
TG	Clock generator

Test circuit



Maximum ratings (all voltages referred to V_{SS})

Supply voltage	V_{DD}	8	V
Input voltage	V_I	−0.3 to 8	V
Current per output	I_O	10	mA
Power dissipation per output	P_O	10	mW
Total power dissipation	P_{tot}	350	mW
Operating temperature	T_{amb}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C

Electrical characteristics T_{amb} = 25°C (all voltages referred to V_{SS})

		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Supply current	I_{DD}	5	12	25	mA
Input current (input without pullup resistors: V_I = 8 V)	I_I		1	10	µA
Input capacitance across V_{SS} (V_I = 5 V; f = 1 MHz)	C_I		5	10	pF

Characteristics of inputs (all voltages referred to V_{SS})

Input signals					
CLK, EO, EU, RA1, RA2, PR, BZ, OZ					
H input voltage	V_{IH}	2		8	V
L input voltage	V_{IL}	−0.3	0.4	0.8	V
H clock pulse width	t_{WH}	0.08			µs
L clock pulse width	t_{WL}	0.08			µs
HL clock transition time	t_{THL}		0.02	0.03	µs
LH clock transition time	t_{TLH}		0.02	0.03	µs
HL transition time for EO, EU	t_{THL}			1	µs
LH transition time for EO, EU	t_{TLH}			1	µs
Input signals					
ST1, ST2, ZK					
Input with pullup resistor					
H input voltage	V_{IH}	2		8	V
L input voltage	V_{IL}	−0.3		0.8	V
H input current (V_{IH} = 8 V; V_{DD} = 4.75 V)	I_{IH}		100	200	µA
L input current (V_{IL} = 0 V; V_{DD} = 5.25 V)	I_{IL}		−25	−100	µA

Characteristics of outputs (all voltages refered to V_{SS})

Output signals					
S1, S2, ACP, AF1 ... AF8					
L output voltage *)	V_{OL}		0.3	0.5	V
Delay time between ACP and AF1 ... AF8	t_{DO}	0.5		2	µs

*) see test circuit

Operating conditions

Detection frequency Lower frequency group at EU	Upper frequency group at EO
f_O = 697 Hz	f_O = 1209 Hz
770 Hz	1336 Hz
852 Hz	1477 Hz
941 Hz	1633 Hz

Frequency detect bandwidth
with S/N = 12 dB : $f_O \pm$ (1.5% + 2Hz)
with S/N = 4 dB : $f_O \pm$ (1.5% + 6 Hz)

Choice of code and scanning with ST1, ST2

	ST1	ST2	Output code
1.	L	H	Binary
2.	H	L	2-out-of-6
3.	L	L	2×(1-of-4)
4.	H	H	no output

ST1, ST2 = H, whenever no potential is applied

Output codes

1. Output in binary code: (output AF1...AF4 and AF7)

Sign	AF1	AF2	AF3	AF4	AF7[1]
1	L	H	H	H	H
2	H	L	H	H	H
3	L	L	H	H	H
4	H	H	L	H	H
5	L	H	L	H	H
6	H	L	L	H	H
7	L	L	L	H	H
8	H	H	H	L	H
9	L	H	H	L	H
0	H	L	H	L	H
*	L	L	H	L	H
#	H	H	L	L	H
A	L	H	L	L	H
B	H	L	L	L	H
C	L	L	L	L	H
D	H	H	H	H	L

2. Output in (2-out-of-6) code: (according to CCITT) (output AF1...AF6 and AF7)

Sign	AF1	AF2	AF3	AF4	AF5	AF6	AF7[1]
1	L	L	H	H	H	H	H
2	L	H	L	H	H	H	H
3	H	L	L	H	H	H	H
4	L	H	H	L	H	H	H
5	H	L	H	L	H	H	H
6	H	H	L	L	H	H	H
7	L	H	H	H	L	H	H
8	H	L	H	H	L	H	H
9	H	H	L	H	L	H	H
0	H	H	H	L	L	H	H
*	L	H	H	H	H	L	H
#	H	L	H	H	H	L	H
A	H	H	L	H	H	L	H
B	H	H	H	L	H	L	H
C	H	H	H	H	L	L	H
D[2]	H	H	H	H	H	H	L

[1] AF7 = carry

[2] Sign D does not exist according to CCITT

3. Output in 2× (1-of-4) code: (output AF1...AF8)

Sign	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
1	L	H	H	H	L	H	H	H
2	L	H	H	H	H	L	H	H
3	L	H	H	H	H	H	L	H
4	H	L	H	H	L	H	H	H
5	H	L	H	H	H	L	H	H
6	H	L	H	H	H	H	L	H
7	H	H	L	H	L	H	H	H
8	H	H	L	H	H	L	H	H
9	H	H	L	H	H	H	L	H
0	H	H	H	L	H	L	H	H
*	H	H	H	L	L	H	H	H
#	H	H	H	L	H	H	L	H
A	L	H	H	H	H	H	H	L
B	H	L	H	H	H	H	H	L
C	H	H	L	H	H	H	H	L
D	H	H	H	L	H	H	H	L

Wiring of the control inputs

Evaluation time Control input BZ
BZ→H short evaluation time (accompanying signal technique)
BZ→L normal evaluation time (speech guard technique)

Output time extension Control input OZ
OZ→H without release time
OZ→L with release time

Output time controller externally Control input ZK
ZK→H Output time is not controllable
ZK→L Output time is not controllable
ZK = H, when potential is not applied

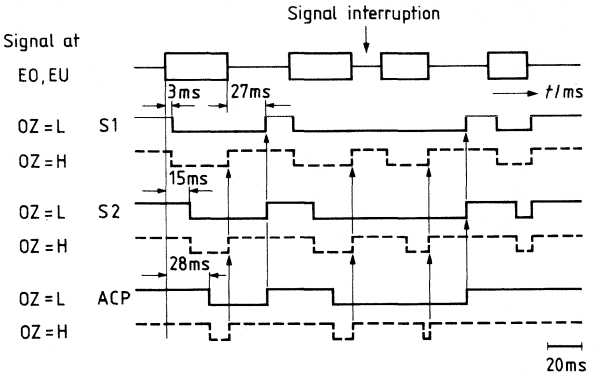
S/N **ratio** Control input PR
PR→H *S/N* – 4 dB
PR→L *S/N* – 12 dB

Access to the guard circuits Control inputs RA1 and RA2
RA1, RA2→H Evaluation will be blocked
RA1, RA2→L Evaluation will not be blocked

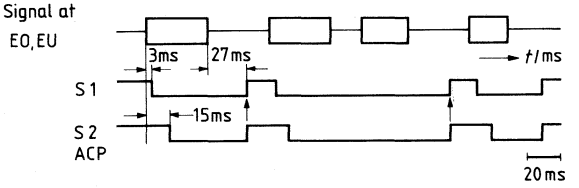
Effectiveness when BZ = L in evaluation range S2 to ACP
BZ = H in evaluation range S1 to ACP

General reset
BZ, OZ→H
PR → L

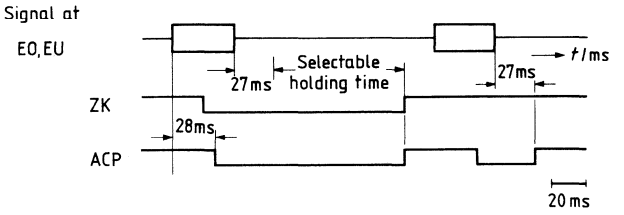
Pulse diagram with BZ = L (normal evaluation time) and ST1 = L



Pulse diagram with BZ = H (short evaluation time) and OZ = L; ST1 = L



Pulse diagram with control of output ACP by means of ZK (in example: (in example: OZ = L; BZ = L; ST1 = L)



Peripheral Board Controller (PBC)

PEB 2050
(SM 205)

Preliminary data

MOS circuit

Type	Ordering code	Package outline
PEB 2050	Q67100–Z157	DIP 40

Features

- Board controller for up to 16 subscribers of a digital switching system
- Designed for different PCM systems
- Time slot assignment freely programmable for all connected subscribers
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides two full duplex PCM highways for the system interface
- System control uses the HDLC protocol with X.25 level 2 functions performed by the PBC
- Standard μP interface
- Two DMA channels for expansion of internal buffer capability of 16 bytes per direction
- μP access to all internal data streams including time slot-oriented data streams
- Support of subscriber circuits by generating timing signals
- Single 5 V power supply
- Low power consumption

General description

The Peripheral Board Controller PEB 2050 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Siemens Codec Filter (SICOFI PEB 2060) it forms an optimized analog subscriber line board architecture. Its flexibility allows the operation as a general purpose controller for data switching and MUX/De MUX applications.

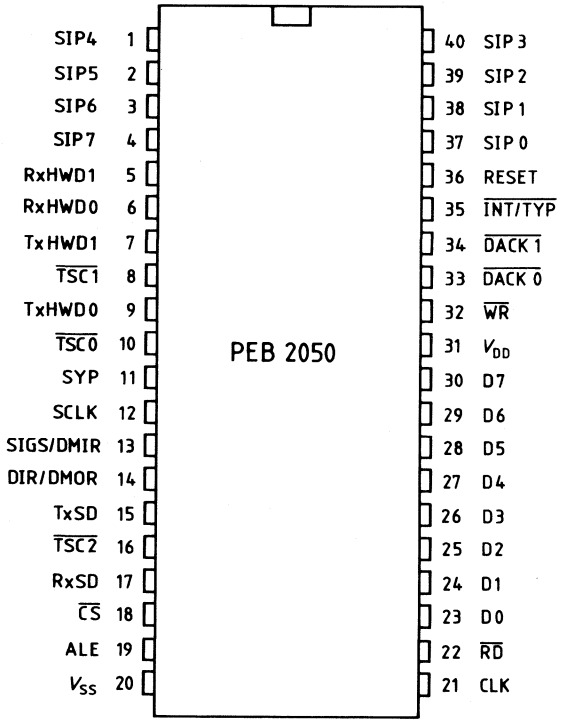
The PBC controls space and time switching functions between subscriber line devices and time division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a processor, which can be an optional line card local processor or the central processor directly. Last, it performs all protocol control functions, using the HDLC protocol format for all information passing between the line card and the central processor via a dedicated HDLC line or via interleaved time slots on the PCM lines.

To meet the different requirements the PBC PEB 2050 provides the following interfaces:

- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and Codec Filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors.
- Double constructed PCM interface.
- Fast serial communication link to the central processor.
- Bit-parallel interface for the connection of 8 bit standard microcomputers such as the SAB 8048. The interface is characterized by an interrupt control and two independent DMA channels, one for the transmit and one for the receive direction.

Pin configuration

top view



Pin designation

Pin No.	Symbol	Name/function	Functional description
1 4	SIP 4 . . . . SIP 7	Subscriber interface port (input/output)	These interface ports are used for bidirectional, bit-serial transfer of speech, data and control words to and from the Siemens Codec Filter (SICOFI) or standard Codec. Corresponding with the direction signal the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 µs frame.
5	R × HWD 1	Receive highway data (input)	Receive PCM highway 1 interface
6	R × HWD 0	Receive highway data (input)	Receive PCM highway 0 interface. The PBC serially receives a PCM word (8 bits) through one of these leads at the programmed time slot.
7	T × HWD 1	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 1 (serial bus). The 8-bit PCM word is serially sent out on this pin at the programmed time slot. Tristate output.
8	$\overline{\text{TSC 1}}$	Tristate control (output, active low)	Normally high, this signal goes low while the PBC is transmitting an 8-bit PCM word on the PCM highway 1.
9	T × HWD 0	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 0.
10	$\overline{\text{TSC 0}}$	Tristate control (output, active low)	Tristate control of highway 0.
11	SYP	Synchronization	SYP is a frame synchronization pulse which resets the on-chip time-slot counters.
12	SCLK	Slave clock (output)	Clock output for the peripheral devices. The signals between the codec filter and the PBC are latched and transmitted with the rising edge of SCLK.
13	SIGS/DMIR	Signal strobe (output, active high)/direct memory input request (output, active high)	The SIGS output supplies a programmable strobe signal. In the DMA mode, this pin is used as DMA input request.

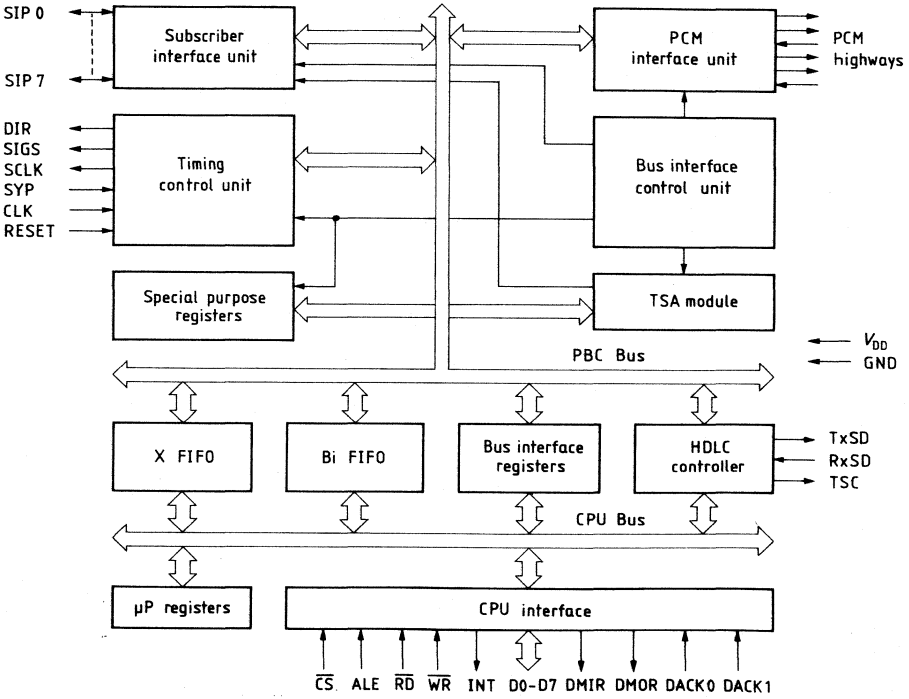
Pin designation

Pin No.	Symbol	Name/function	Functional description
14	DIR/DMOR	Direction (output, active high) direct memory output request (output, active high)	DIR is an 8 kHz symmetric frame signal which controls the direction of the data transfer from and to the peripheral devices. The PBC is able to receive data during the low state of DIR. In the DMA mode this pin is used as DMA output request. DMIR and DMOR are generated by the PBC-internal HDLC receiver or transmitter and are used for handshaking during the DMA transfer.
15	T × SD	Transmit signaling Data (output)	This line transmits the serial data to the dedicated HDLC channel.
16	$\overline{\text{TSC 2}}$	Tristate control to 2 (output, active low)	Normally high, this signal goes low while the PBC is transmitting an HDLC message.
17	R × SD	Receive signaling Data (input)	This line receives the serial data from the HDLC channel.
18	$\overline{\text{CS}}$	Chip select (input, active low)	$\overline{\text{CS}}$ is used to address the PBC. A low level at this input enables the PBC to accept commands or data from a µP within a write cycle, or to transmit data during a read cycle.
19	ALE	Address latch enable (input, active high)	A high level at this input indicates that the data on the external bus is an address selecting one of the PBC-internal sources or destinations. Latching into the address latch occurs during the high low transition.
20	V_{SS}		Ground: 0 V
21	CLK	Clock (input)	A standard TTL clock provides the basic timing of the controller. The clock is synchronous to the PCM clock.

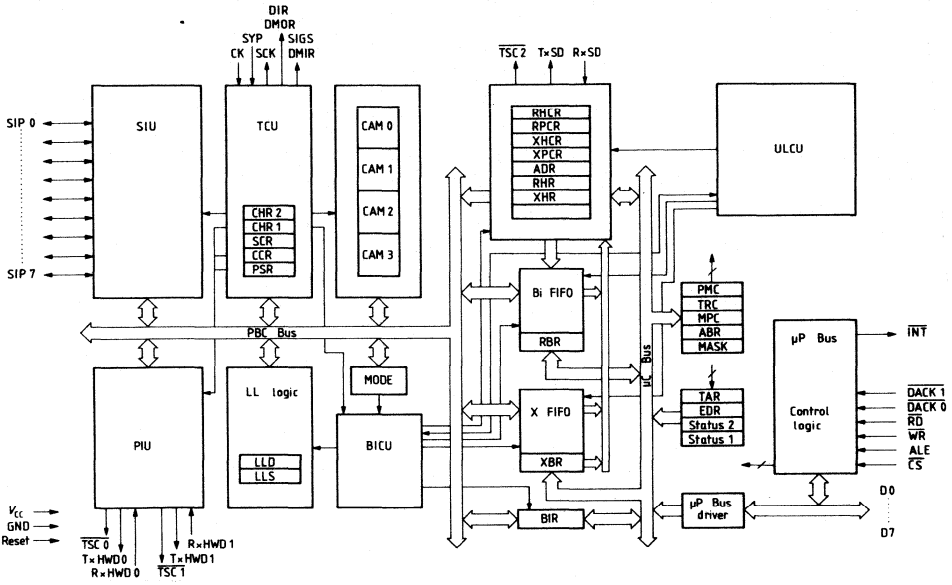
Pin designation

Pin No.	Symbol	Name/function	Functional description
22	$\overline{RD}$	Read strobe (input, active low)	$\overline{RD}$ is used together with CS to transfer data from the PBC to a µP or memory.
23	D0	System data bus	The data bus transfers data and commands between the µP or memory and the PBC.
.	.		
.	.		
.	.		
.	.		
.	.		
30	D7		
31	V_{DD}		Power supply: $V_{DD} = 5.0 \pm 0.25$ V
32	$\overline{WR}$	Write strobe (input, active low)	During the low state of $\overline{WR}$ data can be transferred from the µP or memory to the PBC.
33	$\overline{DACK\ 0}$	DMA acknowledge (inputs, active low)	$\overline{DACK\ 0}$ and $\overline{DACK\ 1}$ are used to acknowledge the DMA output and DMA input request, respectively.
34	$\overline{DACK\ 1}$		
35	$\overline{INT/TYP}$	Interrupt request (output, active low)	This signal is pulled down, when the PBC is requesting an interrupt. In that case the µP should enter into an interrupt routine for reading the status register 1.
36	RESET	Reset (input, active high)	A "high" on this input forces the PBC into reset state. The minimum reset pulse is 16 complete clock cycles.
37	SIP 0	Subscriber interface port (input/output)	These interface ports are used for bidirectional, bit-serial transfer of speech, data and control words to and from the Siemens Codec Filter (SICOFI) or standard Codec. Corresponding with the direction signal the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 µs frame.
.	.		
.	.		
.	.		
.	.		
.	.		
40	SIP 3		

Block diagram



Block diagram



Description of the functional blocks

The PBC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunication system.

Used in peripheral subscriber boards it performs two essential functions:

1) Exchange of control data between a central processing unit, "on board" processing unit and individual subscriber connections. The PBC supports the ISO/CCITT's HDLC communication line protocol. An application specific PBC internal controller controls the distribution of data on the board.
2) The time slot controlled transfer of PCM data (64 Kbaud channels) between the PCM highways and the subscriber connections.

Data transfers between both parts, such as signaling through PCM highways (common channel) or the access of the "on board" µP to 64 Kbaud channels, are considerably simplified by the IC.

The two central functional blocks are reflected in the circuit structure: The PCM synchronous portion constitutes the interfaces to the subscribers and the PCM highways. It comprises the following functional blocks:

- SIU (Serial Interface Unit) with Last Look logic.
- PIU (PCM Interface Unit)
- CAM (Content Addressable Memory)
- TCU (Timing Control Unit)
- MODE register
- PBC Bus

The asynchronous portion constitutes the interface to the local microprocessor (8-bit parallel) and to the central control (serial HDLC interface) and comprises the following functional blocks:

- HDLC controller
- µP interface
- µP control and status register
- ULCU (User Level Control Unit)

The two portions are interconnected by the following functional blocks:

- X FIFO (Transmit FIFO)
- Bidirectional FIFO
- BICU (Bus Interface Control Unit)
- BIR (Bus Interface Register)

Maximum ratings

		Min.	Max.	Unit
Storage temperature	T_{stg}	−65	125	°C

Range of operation

Ambient temperature	T_{amb}	0	70	°C
Voltage at any pin vs. ground	V	−0.3	7	V
Total power consumption	P_{tot}		600	mW

DC characteristics

T_{amb} = 0 to 70°C; V_{CC} = 5 V ± 0.25 V; GND = 0 V

		Conditions	Min.	Typ.	Max.	Unit
L input voltage	V_{IL}		−0.5		0.8	V
H input voltage	V_{IH}		2.0		5.5	V
L output voltage	V_{OL}	I_{OL} = +1.6 mA			0.45	V
H output voltage	V_{OH}	I_{OH} = −400 µA	2.4			V
Input leakage current	I_{IL}	V_{IN} = V_{CC} to 0 V	−10		10	µA
Output leakage current	I_{OL}	V_{OUT} = V_{CC} to 0 V	−10		10	µA
V_{CC} – supply current	I_{CC}	V_{CC} = 5 V		85	120	mA

Capacitance

T_{amb} = 25°C; V_{CC} = GND = 0 V

		Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	f_c = 1 MHz		5	10	pF
Input/output capacitance	$C_{I/O}$			10	20	pF
Output capacitance	C_{OUT}	unmeasured pins returned to GND		8	15	pF

AC characteristics

T_{amb} = 0 to 70°C; V_{CC} = 5 V ± 0.25 V; GND = 0 V

Microprocessor interface

Read cycle

		Min.	Max.	Unit
Address hold after ALE	t_{LA}	20		ns
Address to ALE setup	t_{AL}	30		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
$\overline{RD}$ pulse width	t_{RR}	150	10^7	ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval case 1*	t_{RI}	2 × CP		ns
$\overline{RD}$ control interval case 2**	t_{RI}	100		ns
ALE pulse width	t_{AA}	60		ns

Write cycle

$\overline{WR}$ pulse width	t_{WW}	100		ns
Data setup to $\overline{WR}$	t_{DW}	50		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ control interval case 1*	t_{WI}	2 × CP		ns
$\overline{WR}$ control interval case 2**	t_{WI}	50		ns

* Case 1: Read, write of BI FIFO and X FIFO
** Case 2: All other registers

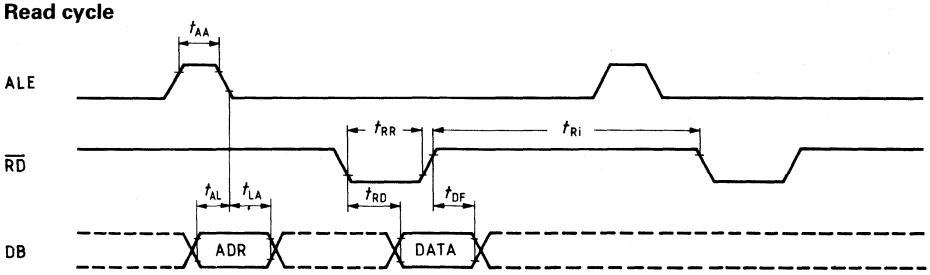
DMA Read		Min.	Max.	Unit
DMA read time*	t_{DMA}		7 × CP	ns
DMOR hold time	t_{DH}		75	ns
Address stable before $\overline{RD}$	t_{AR}	0		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
Output floating delay	t_{DF}	20		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ pulse width	t_{RR}	150	10^4	ns

DMA Write				
DMA Write time*	t_{DMA}		7 × CP	ns
DMIR hold time	t_{IH}		80	ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold after $\overline{WR}$	t_{WA}	0		ns
Data setup to $\overline{WR}$	t_{DW}	30		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ pulse width	t_{WW}	100		ns

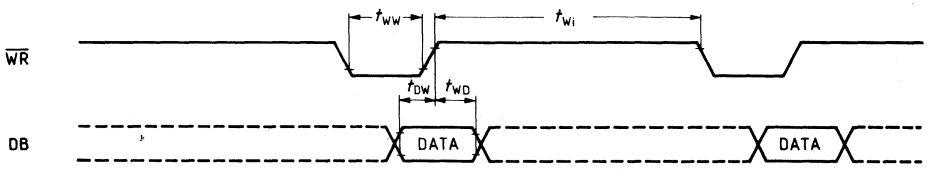
*)

PBC clock/MHz	2.048	4.096	1.536	3.072
2 × CP/ns	980	490	1.300	650
7 × CP/µs	3.4	1.7	4.56	2.3

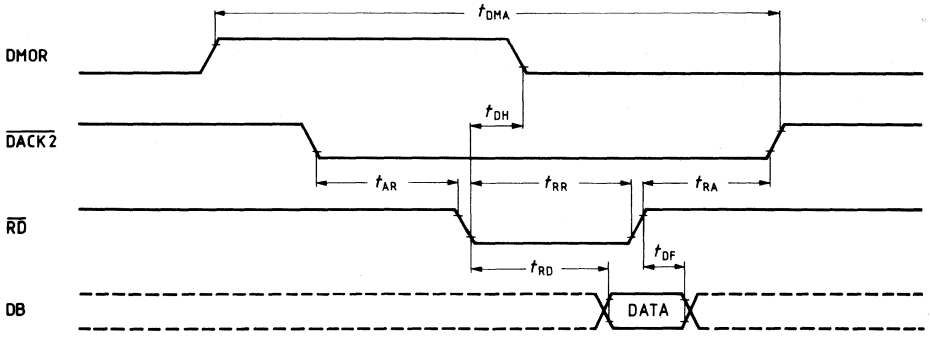
Read cycle



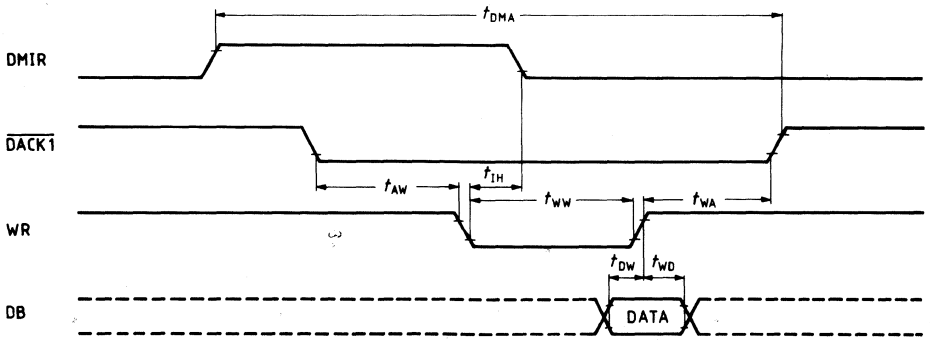
Write cycle



DMA read



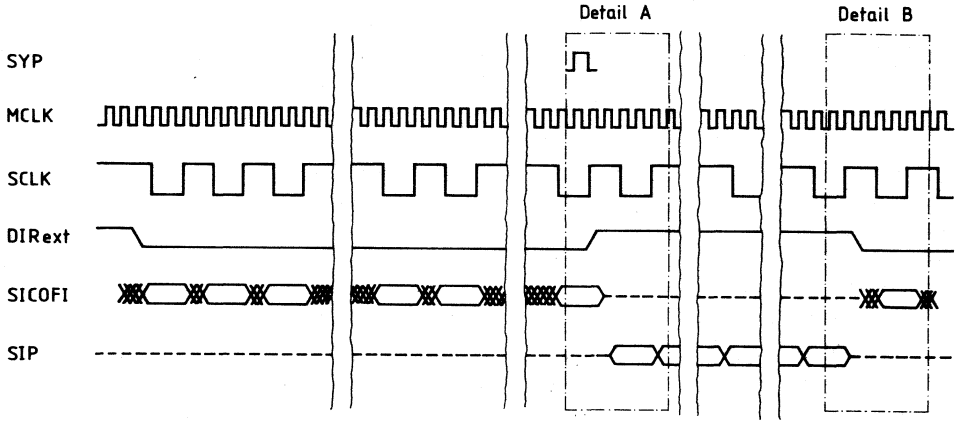
DMA write

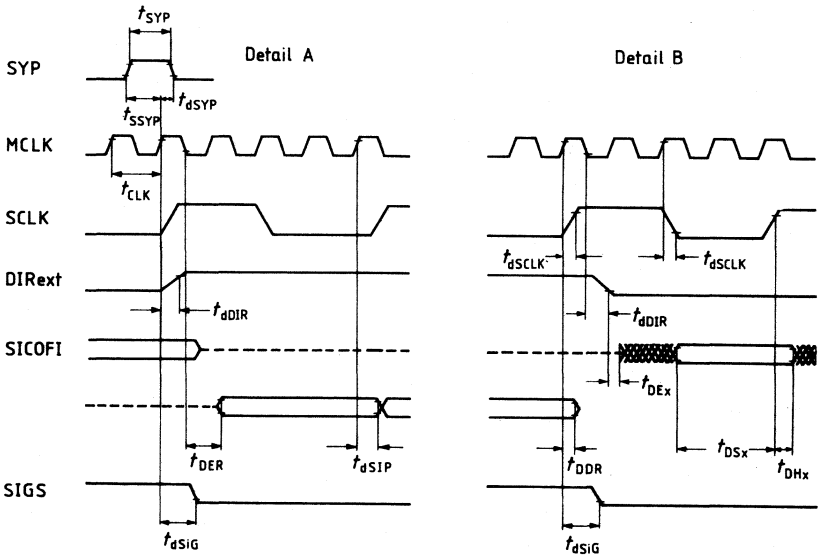


Clock timing

		Min.	Max.	Unit
System clock				
System clock frequency	CLK	1	4.2	MHz
Duty cycle		45	55	%
Synchron pulse period	t_{SPP}	125	M × 125	µs
Synchron pulse width	t_{SYP}	60	t_{CKL}	ns
Pulse delay to CLK	t_{dSYP}	10		ns
Setup time to CLK	t_{sSYP}	50		ns
Clock rise/fall time	CLK_{rf}		10	ns
Slave clock				
Clock frequency	SCLK	512	512	kHz
Clock delay time	t_{dSCLK}	100	165	ns
DIR Clock				
Delay time to CLK	t_{dDIR}	120	190	ns
SIU interface				
SIP data delay	t_{dSIP}	160	300	ns
Data enable receive	t_{DER}	100	180	ns
Data disable receive	t_{DDR}	100	180	ns
Data enable transmit	t_{DEX}	0		ns
Data hold transmit	t_{DAX}	0		ns
Data setup transmit	t_{DSX}	CP/2+200		ns
Signaling strobe delay	t_{DSIG}	110	160	ns

SIP interface timing

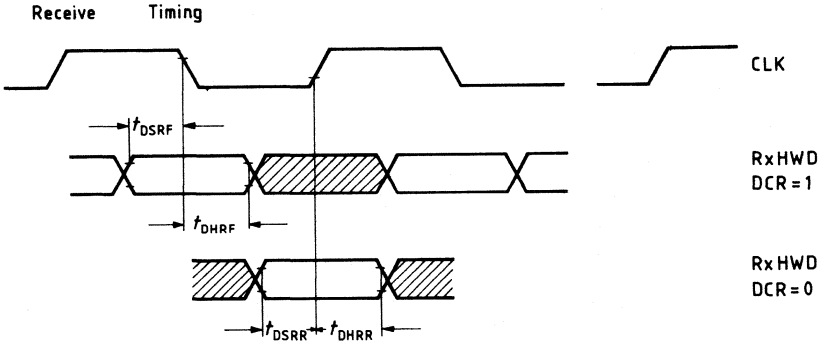




Serial port timing

PCM interface

		Conditions	Min.	Max.	Unit
Receive timing					
Receive data setup DCR = 1	t_{DSRF}		20		ns
Receive data setup DCR = 0*	$t_{DS\,RR}$		40		ns
Receive data hold DCR = 1	$t_{DU\,RF}$		40		ns
Receive data hold DCR = 0	$t_{DH\,RR}$		10		ns



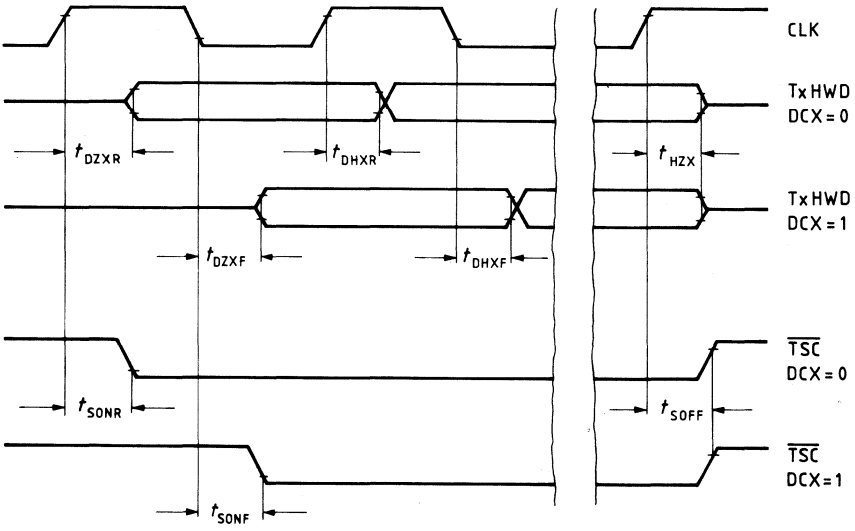
*) Common channel mode t_{DSRR} 60 ns

PCM interface (cont'd)

Transmit timing

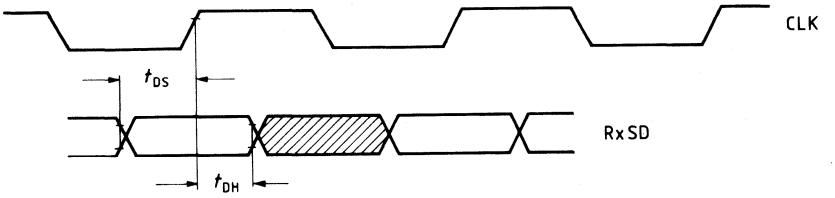
		Conditions	Min.	Max.	Unit
Data enable DCX = 0	t_{DZXR}	C_L = 200 pF	80	160	ns
Data enable DCX = 1	t_{DZXF}	C_L = 200 pF	40	100	ns
Data hold time DCX = 0	t_{DHXR}	C_L = 200 pF	45	160	ns
Data hold time DCX = 1	t_{DHXF}	C_L = 200 pF	40	100	ns
Data float on TS EXIT	t_{HZX}	C_L = 150 pF	35	80	ns
Time slot × to enable DCX = 0	t_{SONR}	C_L = 150 pF	70	130	ns
Time slot × to enable DCX = 1	t_{SONF}	C_L = 150 pF	40	100	ns
Time slot × to disable	t_{SOFF}	C_L = 150 pF	40	100	ns

Transmit Timing

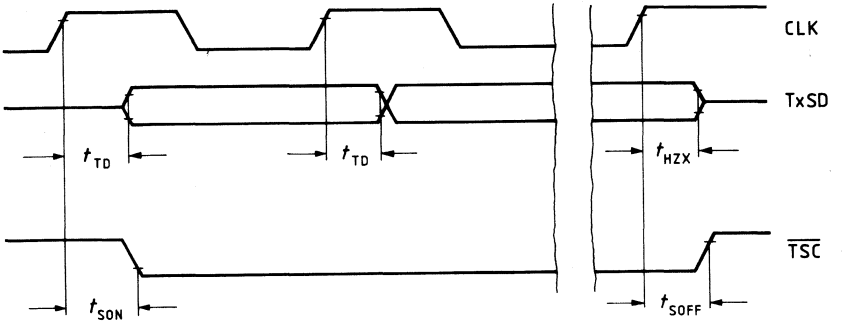


HDLC interface		Conditions	Min.	Max.	Unit
Receive timing					
Receive data setup	t_{DS}		40		ns
Receive data hold	t_{DH}		10		ns
Transmit timing					
Transmit data delay	t_{TD}	C_L = 200 pF	40	100	ns
Data float on TS EXIT	t_{HZY}	C_L = 200 pF	35	80	ns
Time slot × to enable	t_{SON}	C_L = 150 pF	40	95	ns
Time slot × to disable	t_{soff}	C_L = 150 pF	35	90	ns

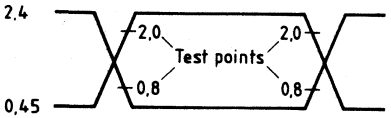
Receive Timing



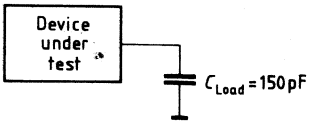
Transmit Timing



AC testing input, output waveform



AC testing load circuit



AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

Siemens CODEC Filter (SICOFI)

PEB 2060 (SM 810)

Advance information

MOS circuit

Type	Ordering code
PEB 2060	Q 67100–Z 153

General description

The Siemens CODEC Filter PEB 2060 is a monolithic CMOS circuit designed for applications in digital exchange telecommunication systems. In combination with the subscriber line interface circuit (SLIC) and the peripheral board controller (PBC PEB 2050) it forms an optimized analog subscriber line board.

After filtering aliasing signals the SICOFI codes the voise signal using a slope adaptive delta modulation loop, yielding an extremely high *S/N* ratio at a sample rate of 128 kHz. The codec signal is subsequently filtered and reduced to a frequency of 8 kHz by a digital signal processor.
Voiceband frequency response and gain are user-programmable through X and GX filters by control words via the DIN/DOUT bidirectional interface. The SICOFI is capable of both A-law and μ-law companding.

In the receive direction the incoming digital signal is first expanded, and then interpolated to a frequency of 256 kHz.

The GR and R filters can be programmed to shape the voice band. With an internal D/A converter and a simple low pass filter the high frequency digital signal is converted to an analog form.

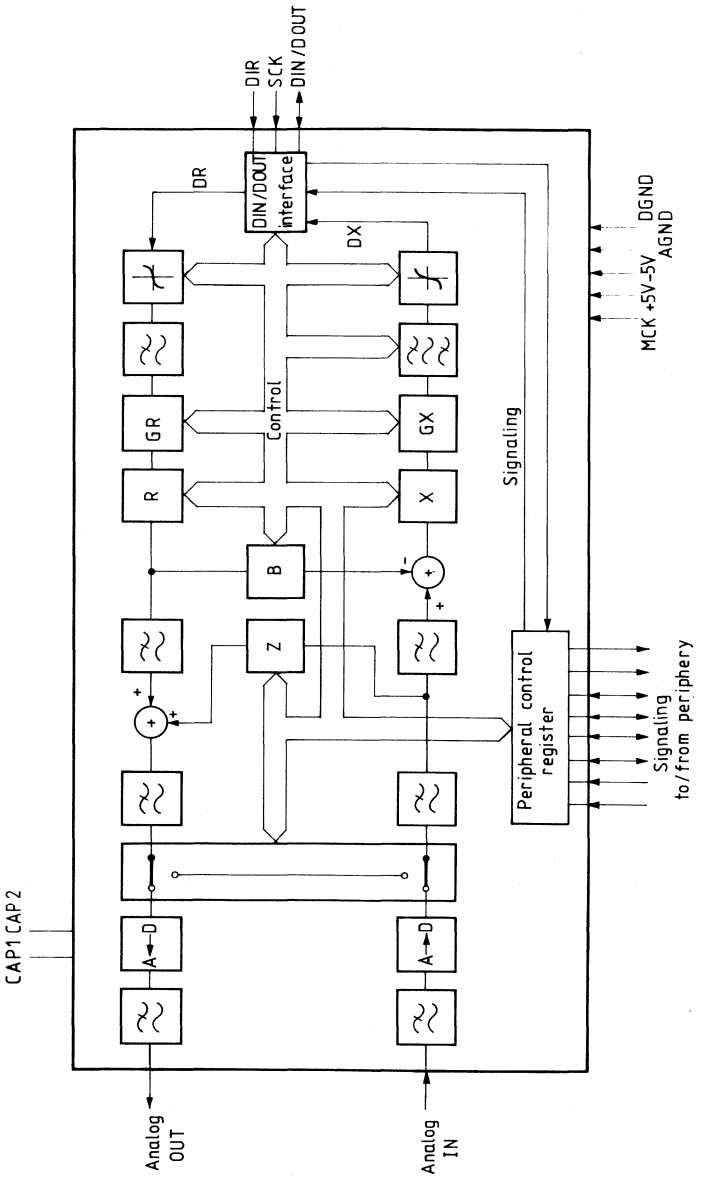
The input impedance can be optimized with the Z filter. With the B filter the 2/4 wire conversion is performed.

All the voice, control and signaling information between the SICOFI and PBC are exchanged on the bidirectional DIN/DOUT line whose direction is controlled by the signal DIR.

Features

- Band limiting
- PCM coding and decoding in A-law or μ-law
- Programmable impedance matching
- Programmable trans-hybrid balancing
- Programmable transfer characteristics
- Programmable internal attenuation
- Programmable interface to periphery (e.g. SLIC)
- Interface to peripheral board controller (PBC PEB 2050)
- 2.048 MHz clock
- Low power CMOS design
- +5V, −5V supply

Block diagram



Memory Time Switch

PEB 2040 (SM 233)

Preliminary data

MOS circuit

Type	Ordering code	Package outline
PEB 2040	Q 67100–Y 669	DIC 40

Features

- Time switch for 2.048 MHz and 8.192 PCM systems
- 16 input PMC lines and speech memory for all 512 subscribers on chip
- Connection memory for 256 channels of 8 output lines on chip
- A time switch with 16/16 PCM lines can be built with two devices
- Non-blocking
- µP interface for writing and reading the connection memory
- Delay between input and output lines selectable
- Tristate for further expansion or hot standby
- Low power
- Single +5V supply

Applications

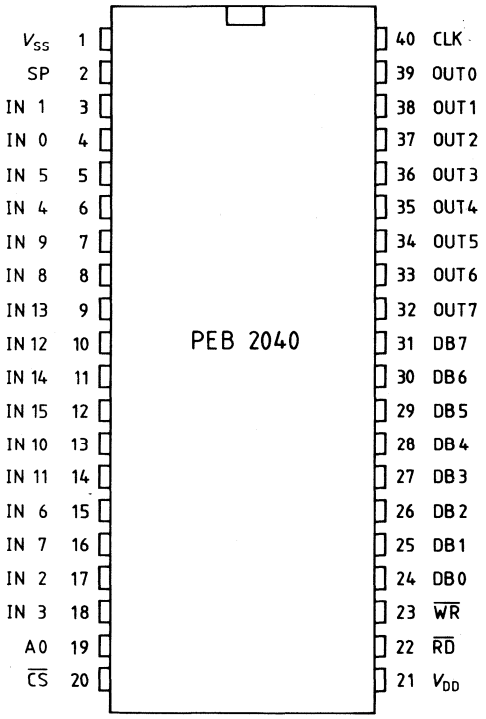
- All types of switching systems
- Complete switch in PCM PABX for up to 512 subscribers with two devices only
- Concentrator function
- Frequency transforming interface between 2 MHz and 8 MHz PCM systems
- 16/16 space switch for 8 MHz

General description

The Siemens memory time switch PEB 2040 is a monolithic NMOS circuit with speech and connection memory on chip. It connects any of 512 incoming PCM channels to any of 256 outgoing PCM channels. Two chips offer a non-blocking 512 channel switch. Block diagrams of 2 PCM systems using the PEB 2040 are shown in **figure 1**. Inputs and outputs are TTL compatible. The total power consumption is 300 mW.

Pin configuration

top view

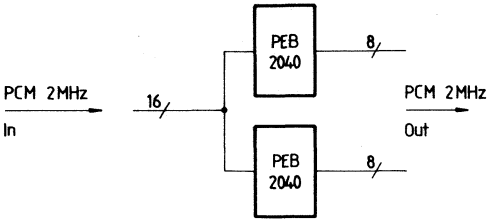


Pin designation

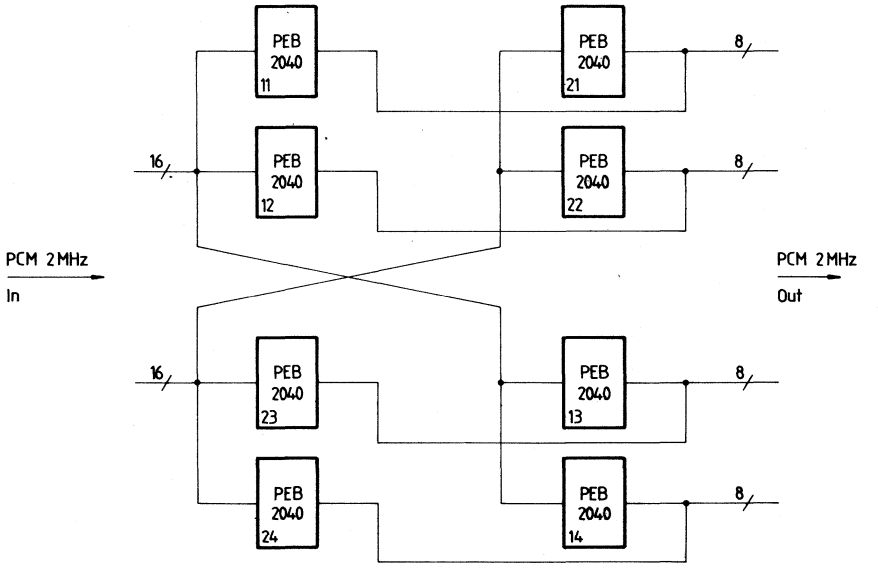
Pin No.	Symbol	Description
1	V_{SS}	Ground (0 V)
2	SP	Synchronous pulse (8 kHz); rising edge for input counter, falling edge for output counter; difference between rising and falling edge should be $\Delta = (2 + n \times 4)\, t_{CL}$ (n = 0–255), rising edge synchronous with the incoming frames; output frame starts 2 clock pulses before the falling edge.
3	IN 1	PCM input port 1
4	IN 0	PCM input port 0
5	IN 5	PCM input port 5
6	IN 4	PCM input port 4
7	IN 9	PCM input port 9
8	IN 8	PCM input port 8
9	IN 13	PCM input port 13
10	IN 12	PCM input port 12
11	IN 14	PCM input port 14
12	IN 15	PCM input port 15
13	IN 10	PCM input port 10
14	IN 11	PCM input port 11
15	IN 6	PCM input port 6
16	IN 7	PCM input port 7
17	IN 2	PCM input port 2
18	IN 3	PCM input port 3
19	A 0 *	Address 0, for separating different modes of the control words
20	$\overline{CS}$ *	Chip select
21	V_{DD}	Supply voltage +5 V ±5%
22	$\overline{RD}$ *	Read pulse
23	$\overline{WR}$ *	Write pulse
24	DB 0 *	DATA Bus 0 }
25	DB 1 *	DATA Bus 1 |
26	DB 2 *	DATA Bus 2 |
27	DB 3 *	DATA Bus 3 } bidirectional
28	DB 4 *	DATA Bus 4 |
29	DB 5 *	DATA Bus 5 |
30	DB 6 *	DATA Bus 6 |
31	DB 7 *	DATA Bus 7 }
32	OUT 7	PCM output port 7
33	OUT 6	PCM output port 6
34	OUT 5	PCM output port 5
35	OUT 4	PCM output port 4
36	OUT 3	PCM output port 3
37	OUT 2	PCM output port 2
38	OUT 1	PCM output port 1
39	OUT 0	PCM output port 0
40	CLK	Clock pulse 8.192 MHz, duty cycle 50%

* µP-controlled interface

Figure 1
Block diagram of two PCM switch configurations with PEB 2040



Memory time switch 16/16 for a non-blocking 512 channel switch.



Memory time switch 32/32 for a non-blocking 1022 channel switch using the tristate function.

Functional description of MTS 16/8

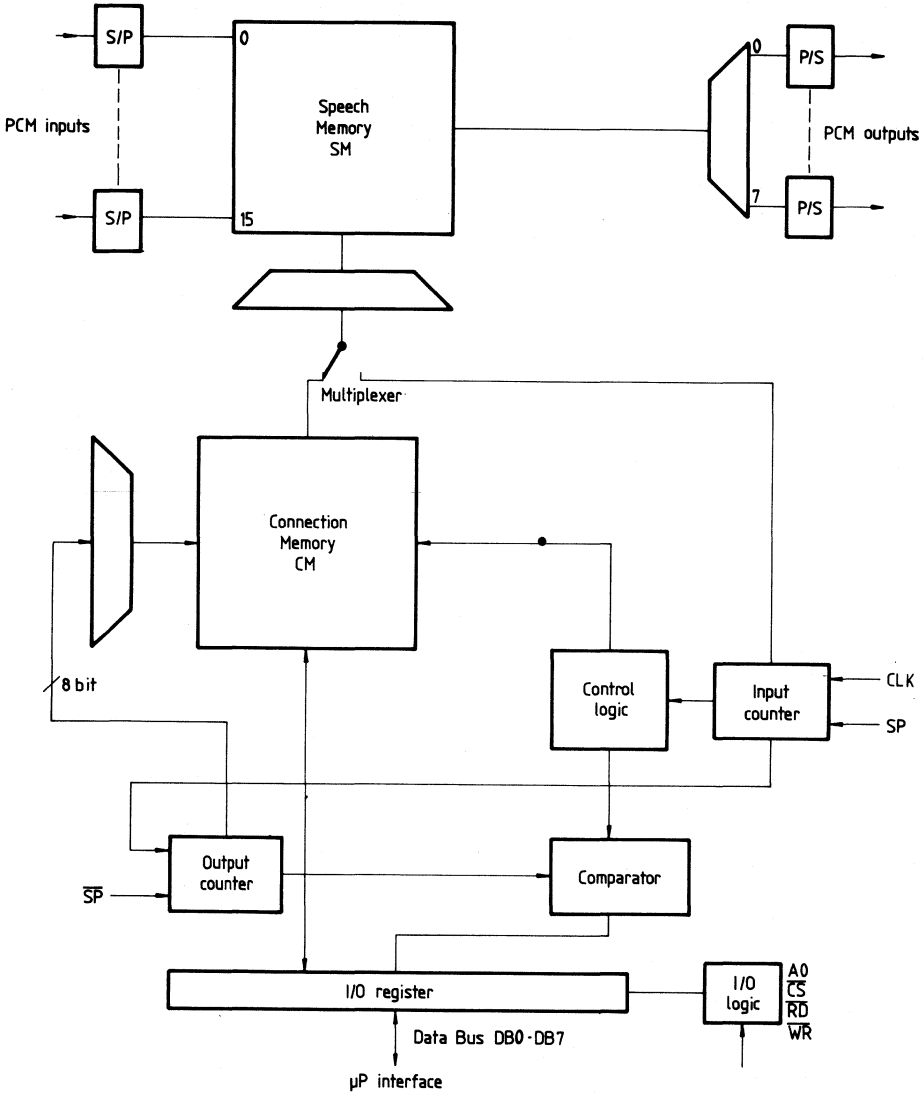
The PEB 2040 is a memory time switch module which has the ability to connect any of the 512 PCM channels of 16 incoming PCM lines to any of the 256 PCM channels of 8 output lines.

A block diagram of the main components is shown in **figure 2**.

The PCM information of a complete frame is stored in the 4K speech memory SM. This means all of the 512 words with 8 bits are written into a fixed position of the SM. This is controlled by the input counter every 125 µs. The words are read with a random access, with an address stored in a connection memory CM for each of the 256 output channels. The access to the CM is controlled by the output counter.

To realize a connection, the SM address and the CM address must be written into the PEB 2040 via a µP interface. The SM address contains the channel and line number of the incoming PCM words. The CM address consists of the channel and line number of the output words.

Figure 2
Block diagram



Operating modes

The PEB 2040 can be connected to 2.048 Mbit/s and 8.192 Mbit/s PCM lines. The "operating mode" is selected by the mode bits, with MI0 and MI1 defining the bit rate of the input lines and independently MO0 and MO1 that of the output lines.

The corresponding input and output addresses are given in **table 1**. The mode MI0 = MI1 = 1 is only for space switch application.

Table 1

Input configuration

PIN No.	MI0=0, MI1=0	MI0=1, MI1=0	MI0=0, MI1=1	MI0=1, MI1=1
	16×2 Mbit/s	4×8 Mbit/s	8×2+2×8 Mbit/s	16×8 Mbit/s
3	IN 1			1
4	IN 0		IN 0	0
5	IN 5			5
6	IN 4		IN 4	4
7	IN 9			9
8	IN 8		IN 8	8
9	IN 13	IN 1	IN 1	13
10	IN 12	IN 0	IN 12	12
11	IN 14	IN 2	IN 14	14
12	IN 15	IN 3	IN 3	15
13	IN 10		IN 10	10
14	IN 11			11
15	IN 6		IN 6	6
16	IN 7			7
17	IN 2		IN 2	2
18	IN 3			3

Output configuration

PIN No.	MO0=0, MO1=0	MO0=1, MO1=0	MO0=0, MO1=1
	8×2 Mbit/s	2×8 Mbit/s	4×2 / 1×8 Mbit/s
32	OUT 7		OUT 7
33	OUT 6		
34	OUT 5		OUT 5
35	OUT 4		
36	OUT 3		OUT 3
37	OUT 2		
38	OUT 1	OUT 1	OUT 1
39	OUT 0	OUT 0	OUT 0

PCM interface

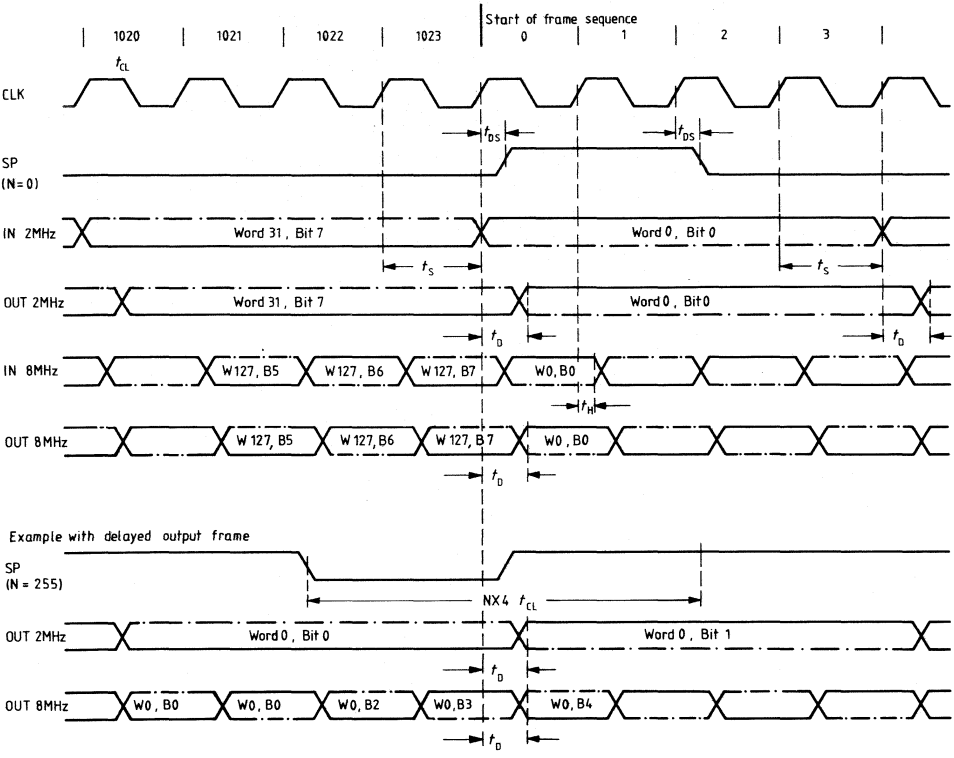
Control signals:
Clock: CLK f_{CL} = 8.192 MHz 50% duty cycle, t_r, $t_f \leqq 10$ ns
synchronous pulse:SP f_{CL} = 8.000 kHz defines the PCM frame with 1024 clock pulses
t_r, $t_f \leqq 10$ ns

PCM input: IN0–IN15
for 2 or 8 Mbit/s, organized as 32 words of 8 bits or 128 words of 8 bits within a frame. The frame for all input lines starts with rising edge of the SP signal.

PCM output: OUT0–OUT7
for 2 or 8 Mbit/s. The frame for all output lines is controlled by the falling edge of the SP signal. The difference between the rising and the falling edge of the SP signal should be $\Delta = (2+N\times4)\ t_{CL}$, $0 < N < 255$. N defines the delay of the output frame counted in 2 MHz bit steps relative to the input frame, as shown in the timing diagram.

The outputs have tristate capability.

MTS 16/8 Timing diagram



t_{CL} = 122 ns
f_{CL} = 8.192 MHz
50% duty cycle

t_{DS} $0 < t_{DS} < 30$ ns
t_S = 120 ns
t_H = 25 ns
t_D = 50 ns (200 pF)

µP Interface DB0–DB7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0

Commands for access to the connection memory, selected by A0 = 1.

All commands have a three-byte structure and must be executed completely.

DB7							DB0	
X	X	K1	K0	X	X	X	S8	Key word
S7	S6	S5	S4	S3	S2	S1	S0	Speech memory address
C7	C6	C5	C4	C3	C2	C1	C0	Connection memory address

Keyword		
K1	K0	
1	0	Write connection memory
0	1	Write connection memory, with checkbytes
0	0	Read connection memory

S8	S7	S6	S5	S4	S3	S2	S1	S0

Speech memory address, stored in the connection memory

C7	C6	C5	C4	C3	C2	C1	C0

Connection memory address

The speech memory address contains the channel and line number of the incoming PCM words. The connection memory address consists of the channel and line number of the output words with the following coordination.

2 Mbit/s input lines	bit 0–3 line number bit 4–8 channel number
8 Mbit/s input lines	bit 0–1 line number bit 2–8 channel number
2 Mbit/s output lines	bit 0–2 line number bit 3–7 channel number
8 Mbit/s output lines	bit 0 line number bit 1–7 channel number

For space switch application with MI0 = 1, MI1 = 1:

8 Mbit/s input lines	bit 0–3 line number bit 4–8 the lower 5 bits of the channel number

Example

Channel 7 of the incoming 2 Mbit/s line No. 9 shall be switched to channel N126 of the output line No. 1 of an 8 Mbit/s system without checkbyte:

Byte			
	0	20 H	(00100000)
	1	79 H	(01111001)
	2	FD H	(11111101)

(0 0 1 0 0 0 0 0) (0 1 1 1 1 0 0 1) (1 1 1 1 1 1 0 1)

Key Word write — Channel 7 — Line 9 — Channel 126 — Line 1

Write connection memory

X	X	1	0	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

A0 = 1, $\overline{WR}$ = 0, $\overline{CS}$ = 0

Stores S8–S0 into the connection memory addressed with C7–C0.

Write connection memory with check bytes desired

X	X	0	1	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

A0=1, $\overline{WR}$=0, $\overline{CS}$=0

Stores S8–S0 into the connection memory addressed with C7–C0.

X	X	0	1	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

A0=1, $\overline{RD}$=0, $\overline{CS}$=0

S8–S0 have been overwritten by the connection memory in the next frame after writing the connection memory.

Read connection memory

X	X	0	0	X	X	X	X
X	X	X	X	X	X	X	X
C7	C6	C5	C4	C3	C2	C1	C0

A0=1, $\overline{WR}$=0, $\overline{CS}$=0

overwrites S8–S0 with the connection memory address C7–C0, and can be read with the following sequence.

X	X	0	0	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

A0=1, $\overline{RD}$=0, $\overline{CS}$=0

Mode/Status selected A0=0
Status A0=0, $\overline{RD}$=0, ($\overline{WR}$=1), $\overline{CS}$=0

DB7							DB0
B	Z	A	0	0	0	0	0

B = 1 Chip busy during command execution
Z = 1 Incomplete command instruction
A = 1 Parity alarm

Parity check DB5 = A

When a speech memory address in written into the connection memory an additional parity bit is generated. With every read access the parity is checked and a violation is latched in the status register from where it can be read by the µP. The reading of the status resets this bit.

Mode A0=0, $\overline{WR}$=0, ($\overline{RD}$=1), $\overline{CS}$=0

DB7							DB0
R	TE	P	SB	MI1	MI0	MO1	MO0

R = Reset — R = 0 Reset
TE = Tristate enable — TE = 0 Mode without tristate function; TE = 1 Tristate dependent on code
P = Parity error — P = 1 Parity error address output
SB = Standby — SB = 1 Tristate independent of code

MI1	MI0	Input operation mode
0	0	16×2 Mbit/s
0	1	4×8 Mbit/s
1	0	2×8+8×2 Mbit/s
1	1	16×8 Mbit/s

for space application only

MO1	MO0	Output operation mode
0	0	8×2 Mbit/s
0	1	2×8 Mbit/s
1	0	1×8/4×2 Mbit/s

Reset

DB7 = R

The PEB 2040 can be initialized by a mode byte with R = 0. This causes the complete connection memory to be overwritten with zeros. During this time the busy bit is set.

Tristate

DB6 = TE, DB4 = SB

The PCM outputs of the PEB 2040 have tristate capability.

1. SB = 1 is a standby mode. All outputs are tristate. The connection memory works in the normal mode.

   The chip can be activated immediately by setting SB = 0.
2. TE = 1, (SB = 0): The output channels are tristate, if the speech memory adress stored in the connection memory is S8–S0 = 0. This means that channel 0 of line 0 is not available for any output.
3. TE = 0, (SB = 0): Channel 0 of line 0 is available, but tristate is not possible.

Parity

DB5 = P

A mode byte with P = 1 causes the latching of the CM address in C7–C0 when a parity violation occurs. This address can be read with a three byte read access. The latched address is the error address n+1.

Operating mode (Input/Output bit rate)

DB0=MO0, DB1=MO1, DB2=MI0, DB3=MI1

The operating mode is selected by the mode bits, where MI0 and MI1 define the bit rate of the input lines and independently MO0 and MO1 that of the output lines.

The corresponding input and output addresses are given in **table 1**.

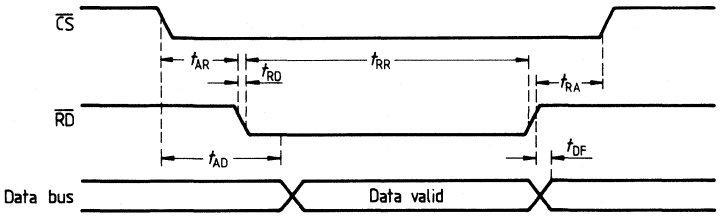
Example

DB7							DB0
1	1	0	0	0	0	0	0

PCM mode: 16×2 Mbit/s input
PCM mode 8×2 Mbit/s output
with tristate

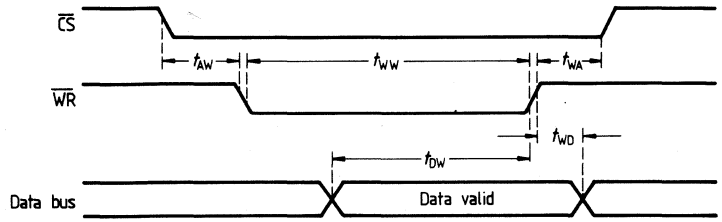
Timing of µP interface

Read operation



		Min.	Max.	Unit
Addr. stable before $\overline{RD}$	t_{AR}	50		ns
Addr. hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	180		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Addr. stable to data valid	t_{AD}		100	ns
Data float after $\overline{RD}$	t_{DF}	10	100	ns
$\overline{RD}$ cycle time	t_{RCY}	500		ns

Write operation



		Min.	Max.	Unit
Addr. stable before $\overline{WR}$	t_{AW}	0		ns
Addr. hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	190		ns
Data setup time	t_{DW}	130		ns
Data hold time	t_{WD}	0		ns
$\overline{WR}$ cycle time	t_{WCY}	500		ns

The "busy time" during which a command or reset instruction is executed has to be programmed with its maximum length or must be controlled via the busy bit of the status register.

Busy time

	Average	Max.	Unit
Reset	188	250	µs
Read connection memory	63	125	µs
Write connection memory	63	125	µs
Write connection memory with check bytes desired	188	250	µs

Maximum ratings

		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	−0.3		7	V
Input voltage	V_I	−0.3		7	V
Total power dissipation	P_{tot}			1	W
Output power dissipation	P_O			10	mW
Operating temperature	T_{amb}	−25		85	°C
Storage temperature	T_{stg}	−55		125	°C

DC and operating characteristics
T_{amb} = −25 to 85°C, V_{CC} = 5 V ± 5%

Supply current	I_{DD}		60	150	mA
Input current	I_I			1	µA
H input voltage	V_{IH}	2.0		V_{DD}	V
L input voltage	V_{IL}	0		0.8	V
H output voltage (I_O = 0.2 mA)	V_{OH}	2.4			V
L output voltage (I_O = 2.0 mA)	V_{OL}			0.4	V
Tristate output leakage V_O = 0 or V_{DD}				1	µA

Subscriber Line Interface Digital (SLID)

PEB 3030 (SM 340)

Preliminary data

MOS circuit

Type	Ordering code	Package outline
PEB 3030	Q67100-Y647	DIC 28

Features

- Digital interface to 4 subscriber lines (time multiplexed burst structure)
- Interface to 2.048 MHz PCM line for 4 × 64 Kbit/s voice or data words
- Interface to 2.048 MHz signaling line for 4 × 2 Kbit/s signaling information
- Alarm generation
- Test with loop back
- Supervision of signaling and synchronization

Application

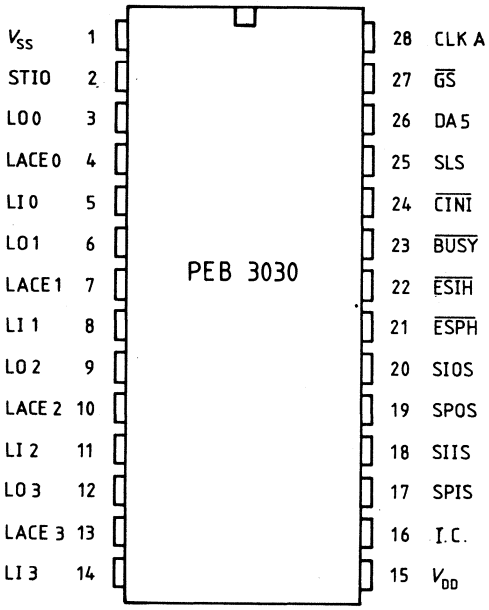
- Interface module of a PCM exchange (PABX) for digital telephone sets or data sets to a PABX
- Interface module of digital concentrators and multiplexers for digital telephone sets

General description

The Siemens subscriber line interface digital (SLID) is a monolithic NMOS circuit. It serves as an interface in a PCM PABX handling up to four digital telephone lines. The 2 wire lines are used in a time multiplexed ("ping pong") mode. A block diagram of a digital telephone system using the SLID PEB 3030 is shown in **figure 1.**

Pin configuration

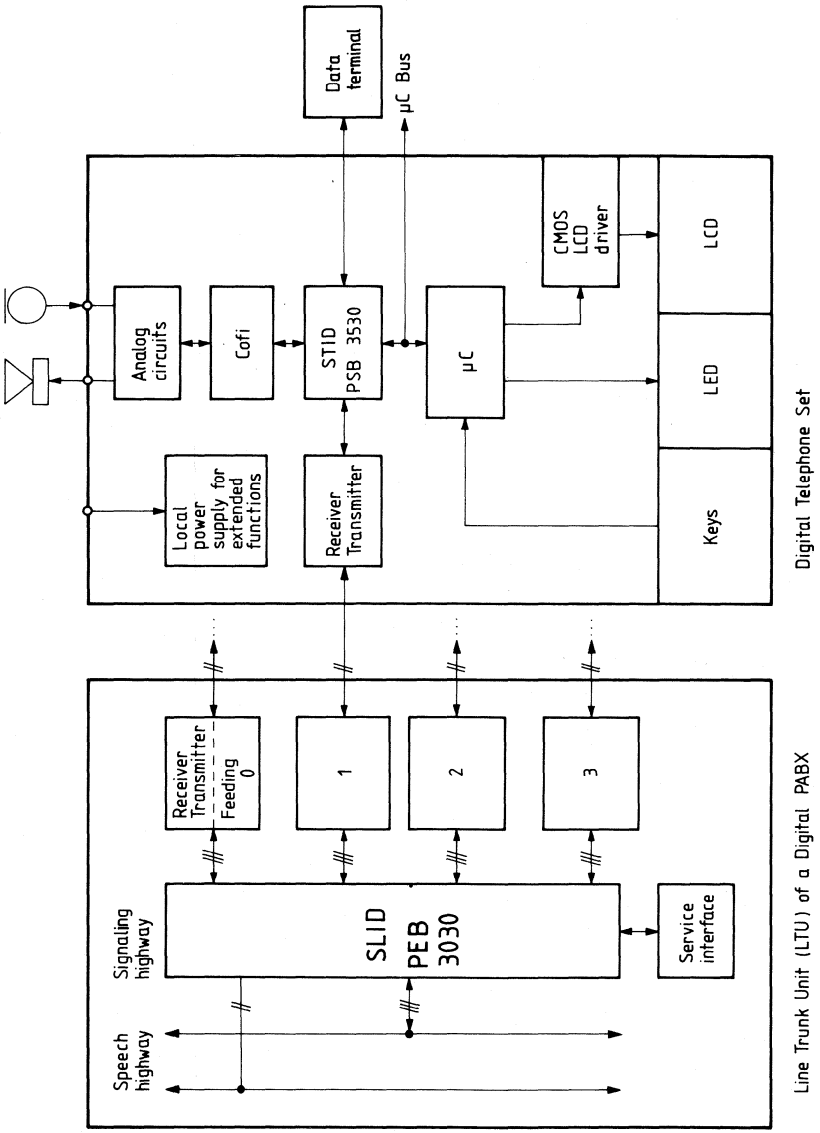
top view



Pin designation

Pin No.	Symbol	Direction	Description	
1	V_{SS}		Ground (0V)	
2	STIO	IN/OUT	Status input/output	
3	LO0	OUT	Line OUT, transmission information	Subscriber 0 SB0
4	LACE0	OUT	Line amplifier control enable	
5	LI0	IN	Line IN, receiving information	
6	LO1	OUT	Line OUT	SB1
7	LACE1	OUT	Line amplifier control enable	
8	LI1	IN	Line IN	
9	LO2	OUT	Line OUT	SB2
10	LACE2	OUT	Line amplifier control enable	
11	LI2	IN	Line IN	
12	LO3	OUT	Line OUT	SB3
13	LACE3	OUT	Line amplifier control enable	
14	LI3	IN	Line IN	
15	V_{DD}		Supply voltage (+5V)	
16	I.C.		Internal connection	
17	SPIS	IN	Speech input subscriber	Interface to system multipl. bus
18	SIIS	IN	Signaling input subscriber	
19	SPOS	OUT	Speech output subscriber	
20	SIOS	OUT	Signaling output subscriber	
21	$\overline{\text{ESPH}}$	OUT	Enable speech highway	
22	$\overline{\text{ESIH}}$	OUT	Enable signaling highway	Interface to operation techn.
23	$\overline{\text{BUSY}}$	OUT	Busy	
24	$\overline{\text{CINI}}$	IN	Calling inhibit input	
25	SLS	IN	Subscriber line select	Interface to SMX control
26	DA5	IN	Device address, superframe signal	
27	$\overline{\text{GS}}$	IN	Group select, signaling channel	
28	CLKA	IN	System clock 2.048 MHz, (duty cycle 50%)	

Figure 1
Block diagram of a digital telephone system



Description of function

Figure 2 shows the block diagram of the SLID PEB 3030 with its interfaces to 4 possible subscribers, to the speech and signaling highways, to the service unit, and to the control interface.

At the subscriber interfaces the PEB 3030 controls the transmission procedure, supervises the sync bits, controls the signaling via "last look" routine, and generates the signaling information in the case of alarms.

Table 1 shows the alarm signaling and the central processor's reaction on special signaling codes. The SLID synchronizes by eliminating the individual line delays, splits, and stores the bursts in the related memory sections.

The LACE signals enable the automatic gain control of the line amplifier.
The signaling and PCM information is then transferred to the related speech- and signaling highways.

At the service interface the busy status is indicated and a service request can be sent to the processor.

All transfer functions of PCM- and signaling information as well as the superframe synchronization are controlled via the control interface by the signals DA5, SLS, $\overline{GS}$, and the 2.048 MHz clock CLKA.

DA5 specifies the 4 ms superframe containing 32 PCM frames. SLS is a pulse with a frame length of 125 µs and a period of 8 frames. Its relative position within the DA5 time corresponds to the 4 time slots of the subscribers within each PCM frame.

$\overline{GS}$ is a pulse with a length of one time slot and determines together with the signal SLS the time slots for the interchange of the signaling information between SLID and signaling highway. **Figure 3 and figure 4** show the timing diagrams for a typical example.

Figure 2
Block diagram of SLID PEB 3030

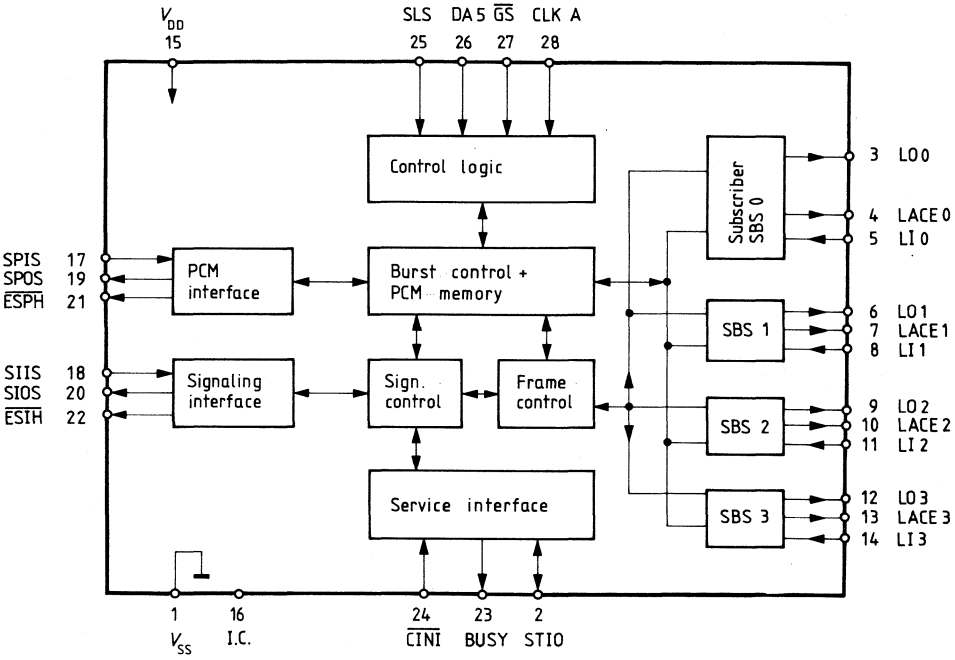


Figure 3

Timing diagram for the system interface (multiplex highway)

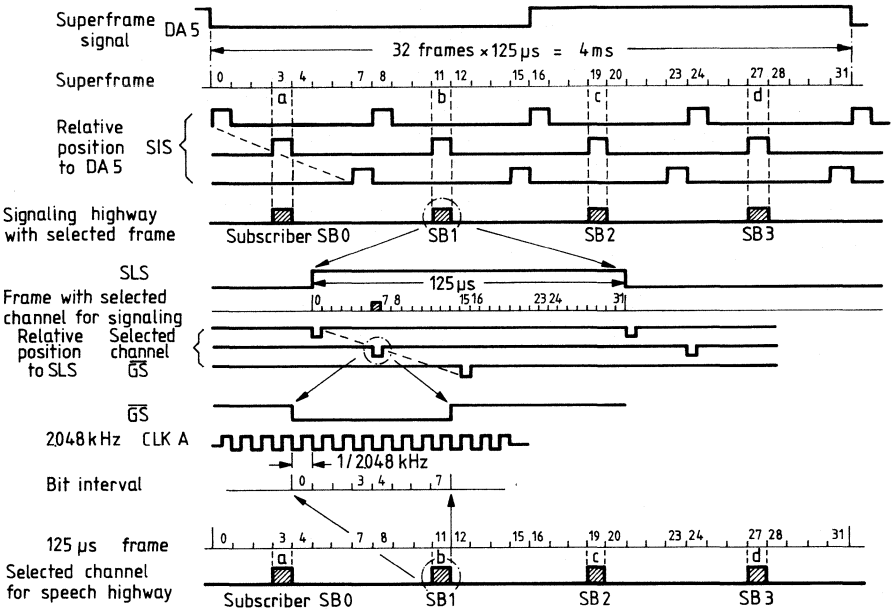


Figure 4

Timing diagram for the transmission on the two-wire subscriber line

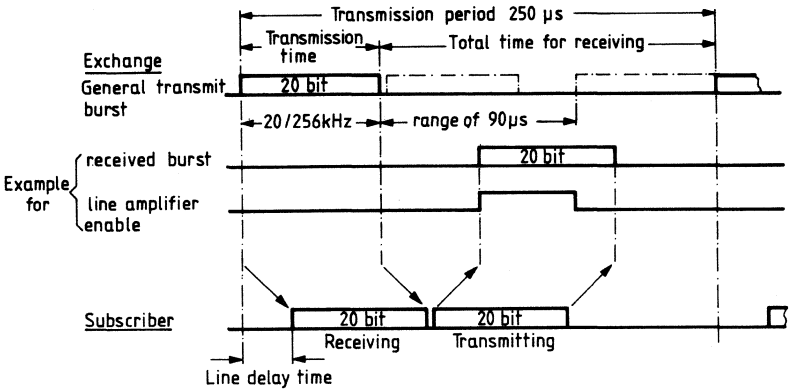
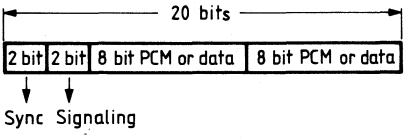


Figure 5

Structure of the subscriber line burst



Synchronization with multi-frame for signaling

Burst period	-- 250 µs
Signaling frame	-- 4 × 250 µs = 1 ms
Signaling bitrate on the line of the digital transmission	-- 8 Kbit / s (8 bit / 1 ms)

Sync	Frame	Signaling
11	1	bit 1,2
10	2	bit 3,4
10	3	bit 5,6
10	4	bit 7,8

Maximum ratings

		Min.	Max.	Unit
Supply voltage	V_{DD}	−0.3	7	V
Input voltage	V_I	−0.3	7	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	−55	125	°C
Total power consumption	P_{tot}		1	W

Electrical characteristics (T_{amb} = 0 to 70°C)

		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Supply current	I_{DD}		40	120	mA
Input current	I_I			10	µA
H input voltage	V_{IH}	2.4			V
L input voltage	V_{IL}			0.8	V
L output voltage	V_{OL}			0.4	V
H output voltage	V_{OH}	3.5			V

Table 1

Special signaling codes

a) Direction from signaling highway to subscriber interface

1.	Busy ON (state) A8 (Hex code)	
2.	Busy OFF (state) A9	
3.	Subscriber – supply ON	AA
4.	Subscriber – supply OFF	AB
5.	SLCD* – test	AC
6.	Line – test	AE
7.	Test – (5 or 6) OFF	AD
8.	End of connection	AF
9.	SLCD* – synchronization routine	B6
10.	Disable subscriber	FF

b) Direction from subscriber interface to signaling highway

1.	Subscriber line disconnected	:02	only by line test
2.	Subscriber line short-circuited	:03	
3.	Subscriber line functional	:00	
4.	Subscriber inactive	:04	no line test
5.	Subscriber asynchronous	:05	
6.	SLCD* asynchronous	:06	
7.	Calling inhibit switch is on	:07	
8.	Signaling last look from subscriber is negative	:00	

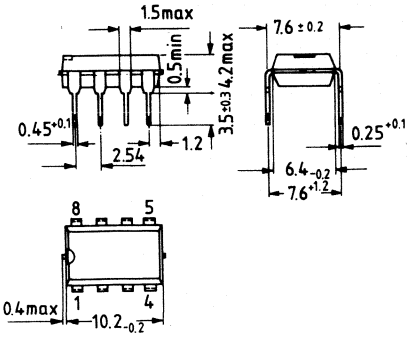
* SLCD = Subscriber line circuit digital

Package Outline Drawings

Package Outlines

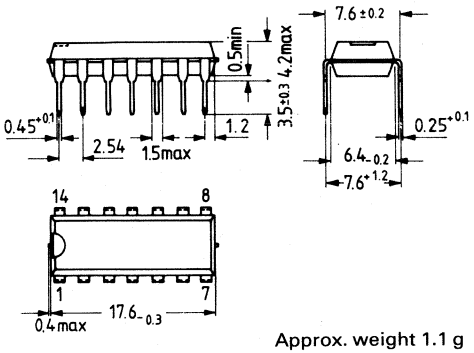
Dimensions in mm

Plastic plug-in package 20 A 8 DIN 41866
8 pins, DIP



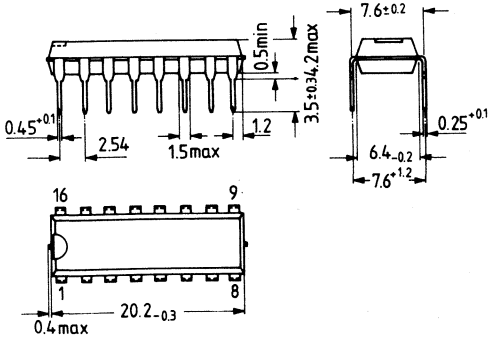
Approx weight 0.7 g

Plastic plug-in package 20 A 14 DIN 41866
14 pins, DIP



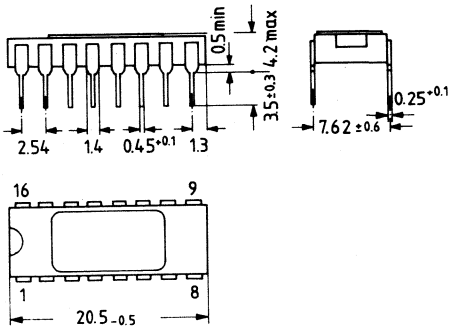
Approx. weight 1.1 g

Plastic plug-in package 20 A 16 DIN 41866
16 pins, DIP



Approx. weight 1.2 g

Ceramic package
16 pins, DIC

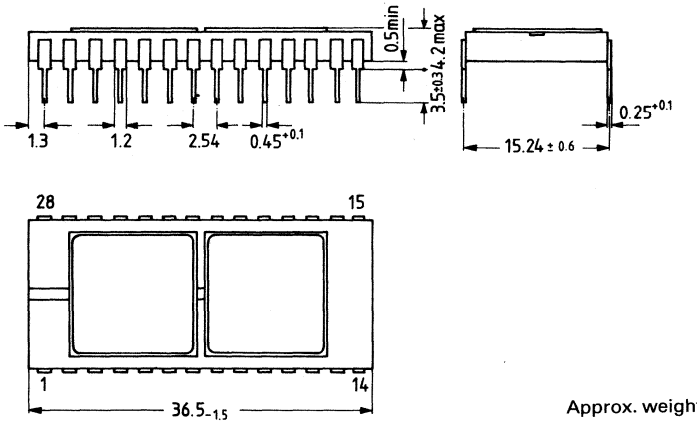


Approx. weight 1.4 g

Package Outlines

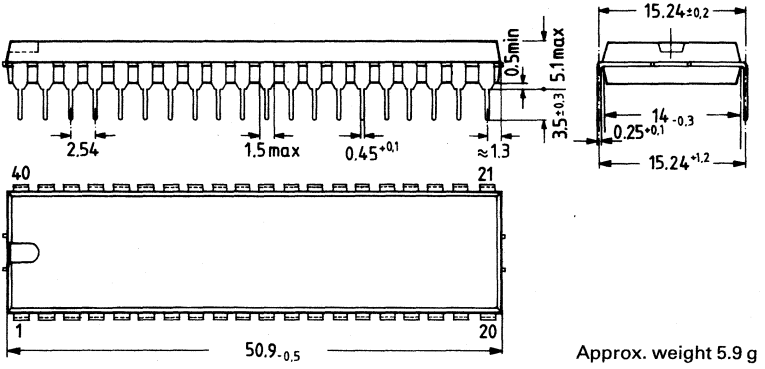
Dimensions in mm

Ceramic package
28 pins, DIC



Approx. weight 3.5 g

Plastic plug-in package 20 B 40 DIN 41866
40 pins, DIP

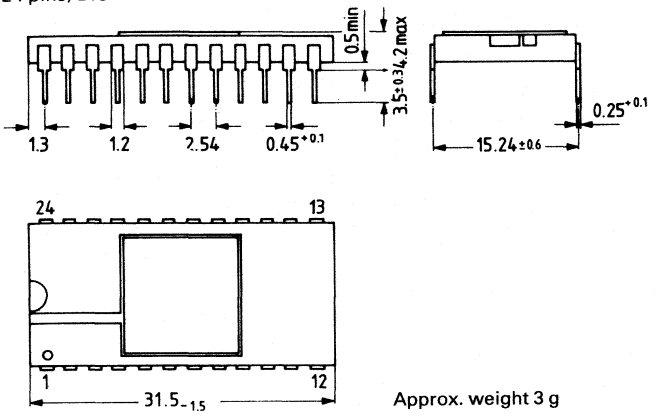


Approx. weight 5.9 g

Package Outlines

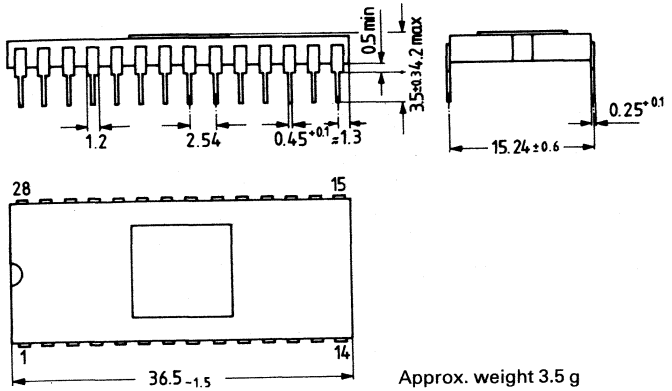
Dimensions in mm

Ceramic package
24 pins, DIC



Approx. weight 3 g

Ceramic package
28 pins, DIC

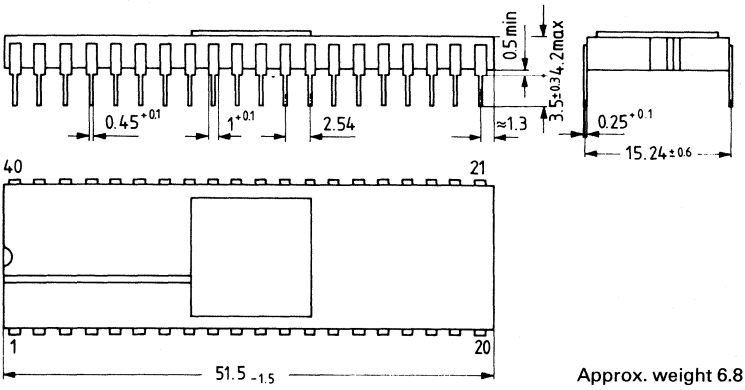


Approx. weight 3.5 g

Package Outlines

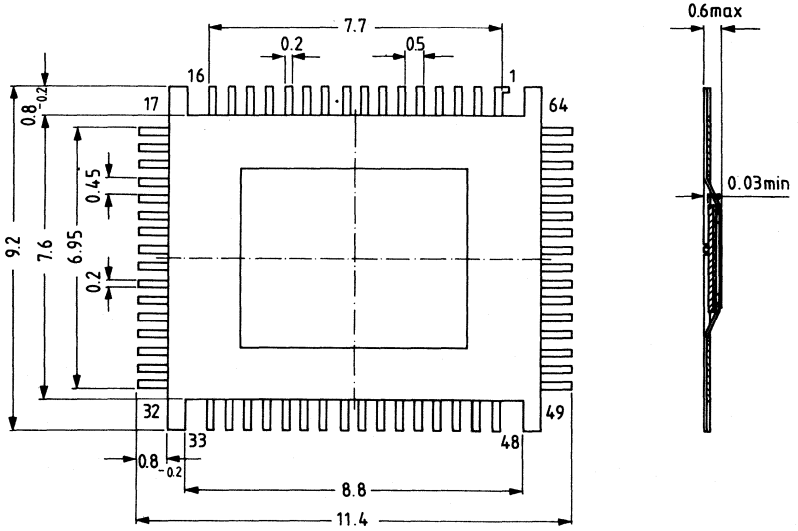
Dimensions in mm

Ceramic package
40 pins, DIC



Approx. weight 6.8 g

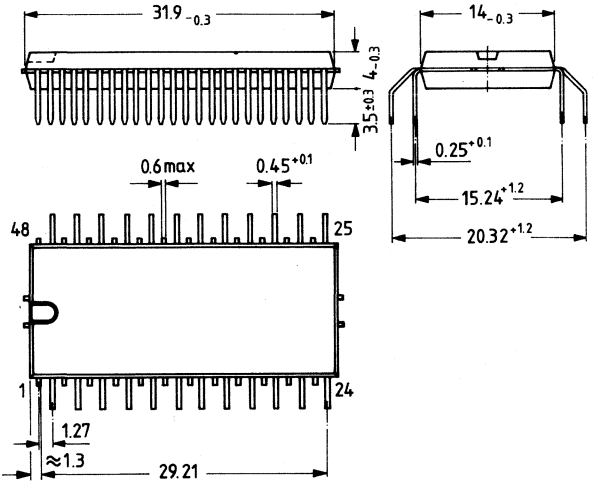
MICROPACK, 64 connections



Package Outlines

Dimensions in mm

Plastic plug-in package
48 pins, QUIP



List of Sales Offices

Siemens worldwide

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34614, 3716

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Switzerland

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☎ (01) 495-3111, Tx 558911

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